

Product Portfolio

February 2016



Leader in CodeChip™ Technology



CodeChips are virtual ASICs. Unlike traditional integrated circuits with fixed features, CodeChips are system-on-a-chip solutions that are integrated onto advanced leading-edge programmable gate arrays. CodeChip's design and feature flexibility allow for lower costs, dramatically faster development cycles, and rapid response to changing requirements. Our CodeChips provide flexible next-generation solutions allowing our customers to meet their growing broadband connection needs.

Cost Savings of an ASIC with Ultimate Flexibility

Arrive is a carrier-class broadband and packet network semiconductor solutions company with a broad portfolio of highly integrated Systems-on-a-Chip products combining voice, data, Internet and multimedia content. Our ASICs and CodeChips™ provide flexible next-generation solutions allowing our customers to meet their growing broadband connection needs.

Arrive Technologies, Inc. was founded and incorporated in 2001, and is principally engaged in development of integrated circuit devices. Its design team is located in Ho Chi Minh City, Vietnam.

Key Product Lines

CodeChip™ Product Line

CodeChips are system-on-a-chip solutions that are integrated onto advanced leading-edge FPGAs. Arrive's flexible CodeChip architecture allows for design changes in real-time, while providing flexibility to accommodate multiple design requirements, adapt to variances in worldwide network standards, and adjust to future technical standard changes—all at a price competitive with fixed-feature ASICs. PCB size, BOM, and power consumption are also reduced by the Arrive CodeChip architecture.

The CodeChip family begins with a series of core features. From these, each specific design is built to customer specifications.

There are currently four CodeChip families:

- Pseudowire CodeChips
- SONET/SDH CodeChips
- Carrier Ethernet CodeChips
- Multi-Services OTN and CPRI over OTN CodeChips

Arrive is also currently developing a new family of Next Generation CodeChips™. This new family will provide a rich menu of FPGA-based IP to accelerate CPU performance for SDN/NFV applications.

The CodeChip Advantage

CodeChip is more than just IP blocks for FPGAs. An Arrive CodeChip includes the full FPGA Image, a full software development kit including APIs and Drivers, and is backed by the world-class integration and testing experience of Arrive. Many customer applications require combinations of these product lines, and Arrive has the experience to combine these solutions effectively.

Multiservice ADM ASIC Product Line

Arrive also specializes in high capacity ASIC devices. Arrive's AT4848 is a highly integrated OC-48/STM-16 or OC-12/STM-4 or OC-3/STM-1 Multiservice ADM (Add/Drop Multiplexer) on a chip. Devices in this family can be used in a variety of voice and data over SONET/SDH systems including Multiservice Provisioning Platforms (MSPP), broadband access and enterprise customer premise equipment with an integrated ADM.

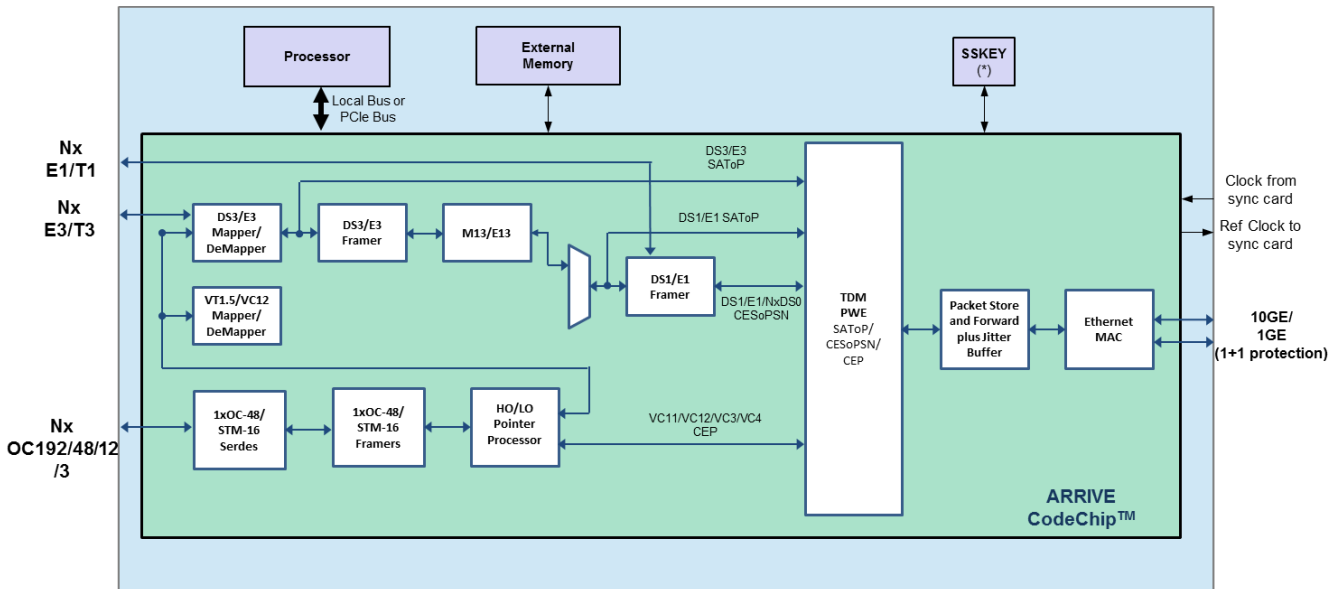
Pseudowire CodeChips

Arrive's Pseudowire CodeChip product line offers a family of complete pseudowire and mobile backhaul CodeChip devices. Arrive provides total solutions in groupings of 1 to 32 E1/DS1/J1 lines; aggregation nodes with up to 84/63 DS1/E1 lines; high-density nodes with 336/252 DS1/E1 or OC-12/STM-4 lines; or very dense nodes with 5376/4032 DS1/E1/J1 or 1xOC192/STM-64 - 4xOC48/STM16 lines. The aggregation and higher density nodes use SONET/SDH interfaces for service side connection. The Pseudowire CodeChip family is described in more detail on the Arrive website.

Pseudowire CodeChip Applications

- Metropolitan Area Network Aggregation
- PON, Cable and Wimax backhaul systems
- Gateway of Pseudowire and voice trunking
- Aggregation of Packet Mobile Backhaul
- Metro Ethernet Equipment
- TDM and LAN aggregation

High Channel Count Pseudowire CodeChip Block Diagram



Pseudowire CodeChips - Key Features

- SAToP/CESoPSN/TDMoIP/MEF8 Circuit Emulation Services for E1/T1/E3/T3
- Circuit Emulation over Packet (CEP) for OC3/12/48
- Timing modes for DS1/E1 include: ACR/DCR, EPAR/APM, external reference, looptime
- ACR/DCR clock recovery algorithm for SAToP and CESoPSN, per ITU G.8261, G.823, G.824 and MEF22
- Very low-cost DDR2/3 for large buffers
- Application-specific high-level API software development kit

E1/T1/E3/T3 Pseudowire CodeChips

- Supports up to 63 E1/T1 or 24 E3/T3 pseudowires over packet switched network (SAToP/CESoPSN), ATM pseudowire and packet pseudowire as per RFC4553 and RFC5086
- Intergrated PDH Framers with M13
- 1+1 GbE Interface for network side

STM-1/OC-3, STM-4/OC-12, and STM-16/OC-48 Pseudowire CodeChips

- Supports up to 1xOC192/STM-64 - 4xOC48/STM16 or 5376/4032 DS1/E1/J1
- PDH pseudowire (CES: SAToP and CESoPSN) as per RFC4553, RFC5086, etc.
- SONET/SDH pseudowire (CEP) as per RFC4842
- DS1, E1, J1, DS3, E3, with optional M13/E13
- CEP modes include: VC11, VC12, VC-3 (Basic and Fractional), VC-4 (Basic and Fractional)
- High channel count pseudowire connections with NxDS0 capability
- OC12/STM-4 or OC-3/STM-1 interfaces at service side
- DS1, E1, J1, DS3, E3, with optional M13/E13
- GbE interfaces: One active and one standby
- APM and EPAR Timing modes for CEP

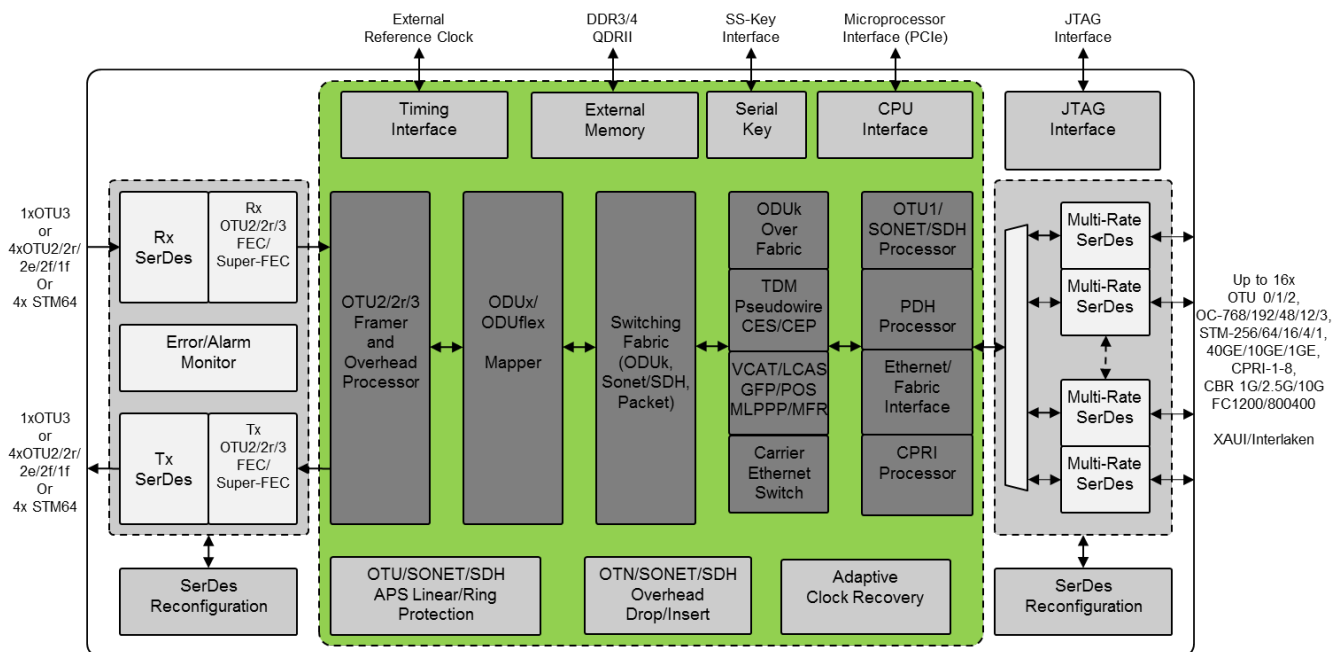
Multi-Services OTN CodeChips

Arrive's Multi-Services OTN CodeChip offers up to a 40Gbps OTN processor, with highly integrated capabilities for SONET/SDH, CES/CEP, and Carrier Ethernet features. The network side can support multiple OTU rates (OTU3/OTU2/OTU2r/OTU2f/OTU2e/OTU1f) and 16 transceivers on the client side can be configured with various protocols: SONET/SDH, 1GE/10GE/40GE, Fiber Channel, ESCON/FICON, CPRI, CBR or XAUI/Interlaken for OTN-over-Fabric.

The Multi-Services OTN CodeChip can be used in a pizza-box or system linecard for OTN Transponder/Muxponder/ODUk Switching or P-OTS with additional customer-defined functions.

A variation of the OTN CodeChip can be used for CPRI-over-OTN in a small size FPGA. This CodeChip provides high quality frequency and very low latency that can provide a cost effective solution for next generation C-RAN Mobile Fronthaul while still meeting the strict timing requirements of CPRI and 3GPP.

Multi-Services OTN CodeChip Block Diagram



Multi-Services OTN CodeChip Key Features

OTN Features

- 40Gbps with 1xOTU3 or 4xOTU2/2r/2e/2f/1e/1f at Network Side
- Up to 16 client ports with up to 10Gbps, multiple protocols support:
 - OTU0/OTU1/1e/1f/OTU2/2r/2e/2f
 - SONET/SDH: STM-256/64/16/4/1 – OC768/192/48/12/3
 - 40G/10G/1G Ethernet
 - CPRI option 3-8
 - CBR 1G/2.5G/10G
 - XAU/Interlaken
- AES-256 Data Encryption/Decryption for OTN traffic or MACSec, IPSec
- Support CPRI over OTN with multiple mapping: G.Sup56, GFP-T

Integrated Features

- Integrated SONET/SDH MSPP with VCAT/LCAS, GFP/HDLC/MLPPP/Multi-Frame Relay
- Integrated high capacity, deep channelized for lo-order SONET/SDH and PDH processing
- Integrated High-order/Low-order CES/CEP
- Integrated L2/MPLS Switch with OAM/1588v2/SyncE

Target Applications

- Multiservice line-card for OTN Metro Access Network
- Reconfigurable Add-Drop Multiplexers (ROADMs)
- CRAN – OTN Mobile Fronthaul
- OTN Transponder/Muxponder/Switching/P-OTS

SONET/SDH CodeChips

Arrive's SONET/SDH CodeChip product line offers a family of highly integrated SONET/SDH Framer/Mapper products that can be used in Linear or Ring topology SONET/SDH networks. They can support typical transport configurations, including PDH-over-SONET/SDH, Ethernet-over-PDH, Ethernet-over-PDH over-SONET/SDH, Ethernet-over-SONET/SDH, SONET/SDH ADM, SONET/SDH MSPP.

The SONET/SDH CodeChip family begins with a series of core features based on the proven AT4848 ASIC and other devices. From these, each specific design is tailored to a customer's specifications. Following are several example configurations; the family of devices is described in more detail on the Arrive website.

SONET/SDH CodeChip Key Features

Core	Bandwidth	Key Features
SONET/SDH and/or PDH ADM	16Mbps (8xE1/T1) to 20Gbps (2xOC192 or 8xOC48)	<ul style="list-style-type: none"> • Linear ADM , 1+1 MSP , UPSR/SNCP • Cross-connect • Full PDH (E3/T3/E1/T1) framer • Ethernet over SONET with LCAS/VCAT
SONET/SDH EoS/EoPDH/POS	155Mbps (OC3) to 20Gbps (2xOC192 or 8xOC48)	<ul style="list-style-type: none"> • Channelized Ethernet over TDM (EoS, EoPDH) VCAT-LCAS, GFP/HDLC • Packet over SONET/SDH (POS)
SONET/SDH MSPP	155Mbps (OC3) to 10Gbps (1xOC192 or 4xOC48)	<ul style="list-style-type: none"> • Full SONET/SDH features • Full PDH features • PPP/MLPPP/Frame Relay/ Multi-Frame Relay • ATM/IMA

Carrier Ethernet CodeChips

Arrive's Carrier Ethernet CodeChip devices offer Packet Processing, Switching, Routing targeted with different capacities, I/O, features and cost to meet the varied needs of equipment suppliers.

The Carrier Ethernet CodeChips can be used on various packet system line cards and pizza-box systems for optical packet transport and packet radio transport. Broad applications include wireline networks and wireless networks. Many specific applications are possible, such as IP/MPLS, WDM-PON, FTTH, wholesale Ethernet, LTE, 3G and 4G backhaul, microwave radio backhaul, eNodeB and RT.

Carrier Ethernet CodeChips, Bandwidth Specific Features

CodeChip	8-24G	24-40G	80G
Switching Capacity	Up to 24Gbps	Up to 40 Gbps	Up to 80Gbps
10 GbE Ports	1 or 2, XAUI or 10GBASE-R/KR	1 or 4, XAUI or 10GBASE-R/KR	1 or 8, XAUI or 10GBASE-R/KR
GbE Ports	Up to 24	Up to 32	Up to 32

Carrier Ethernet CodeChips, Key Features

- L2/MPLS/MPLS-TP Switching and L3 IPv4/IPv6 Routing
- Support Hierarchical QoS (H-QoS) for flexible per flow/per service Traffic Manager or simple QoS (8 queues/port) for smaller size FPGA.
- Optional MACSec/IPSec security
- TWAMP hardware acceleration
- OAM Modes:
 - IEEE 802.1ag/ ITU-T Y.1731 CFM (Connectivity Fault Management) OAM with hardware acceleration engine
 - CFM/BFD OAM with hardware acceleration for MPLS-TP
 - IEEE 802.3ah EFM (Ethernet in the First Mile) OAM
- Sub-50ms protection switching times
- Protection Modes:
 - Ethernet Linear Protection Switching 1+1, 1:1 (G.8031)
 - Ethernet Ring Protection Switching (G.8032)
 - MPLS Linear/Shared Ring protection
 - Ethernet link aggregation (IEEE 802.3ad)
 - Spanning tree (STP), Rapid spanning tree (RSTP)
- IEEE 1588v2
- G.8262/Y.1362 Synchronous Ethernet (SyncE)
- Optional support via a companion FPGA:
 - CES, CEP
 - ATM/IMA
 - PPP/MLPPP
 - EoS, EoPDH

CodeChip SDK (Software Development Kit)

All Arrive CodeChips come with a Software Development Kit. Major features are:

- Platform independent via a Hardware Abstraction Layer (HAL) module
- Operating System independent via Operating System Abstraction Layer (OSAL) module
- Modular device driver allowing transparent interface to higher level application layer
- Relieves the system software developer of the task of recreating the CodeChip device driver to speed up the system development and ensure a quick transition to production
- Compliant to standard telecommunications functions including configuration
- Supports interrupt handler
- Includes a command line debugger for controlling and monitoring the device
- Compliant to ANSI-C

EVALUATION PLATFORMS

Arrive has developed evaluation platforms for the CodeChip and Multiservice ADM ASIC products. These platforms are designed to allow prospective customers to comprehensively test and evaluate Arrive's solutions and for existing customers to develop applications software prior to their own hardware becoming available.

EP5/EP6s are standalone boards that allow operation and interoperability testing of the different CodeChip families through various interfaces. User manuals provide an overview of the capabilities and features of the EP5/EP6 boards. Evaluation and testing can be controlled via a 10/100BT Ethernet port which is connected to the onboard CPU by either a PC or a LAN. A standard RS-232 debugging port is also provided.



For more information on Arrive's Codechip and ASIC solutions, please visit our website at

www.arrivetechologies.com

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