

INTRODUCTION

The Thalassa platform offers solutions for high capacity Pseudowire Emulation applications for DS3/E3, DS1/E1, NxDS0 CES channels, SONET/SDH channels or ATM/FR/HDLC/PPP/Ethernet traffic over Packet Switched Networks (PSN). It can be used in any application requiring Pseudowire emulation over PSNs including wireless backhaul, circuit, cell or packet business private line transport, TDM over PON, Cable or WiMax or any multi-service transport over/through a MPLS, Metro Ethernet or IP PSN.

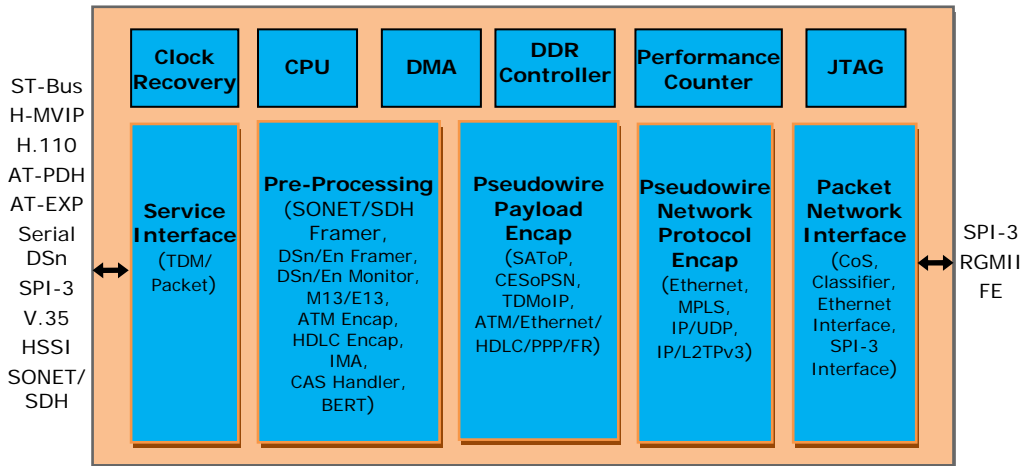
The platform includes flexible I/O on the TDM/Service side including ST-Bus, H.110, H-MVIP, AT-DS0 for nxDS0, AT-VT Bus for carrying VT/TUs, DS1/E1/serial ports, DS3/E3 high speed serial ports, an AT-PDH bus, Parallel SONET/SDH ports, V.35 serial ports, HSSI serial ports and SPI-3 packet interface. On the PSN side, it includes MACs for direct Ethernet (FE, GE) and a SPI-3 to interface with a Network Processor, Carrier Ethernet switch or external MAC devices. The Thalassa supports TDM CES for structure aware and structure agnostic architectures including AAL1, AAL2 CESoPSN and SAToP plus TDM CEP (SONET/SDH) for SONET/SDH over PSN and packet/cell modes for Frame Relay, HDLC/PPP, ATM and Ethernet payloads. Thalassa provides rich timing and clock recovery capabilities plus OAM/Diagnostics and flexible packet encapsulation for MPLS, Metro Ethernet and IP L2TP Networks.

Arrive's Thalassa is targeted at FPGA based implementations. This approach allows upgrade protection for evolving standards and a very quick time to market while avoiding expensive single sourced NPUs and the risk of selecting a feature frozen ASSP. The Thalassa platform is a collection of powerful building block functional elements that can be quickly assembled into an FPGA allowing Arrive to quickly provide a wide range of variations fitting any application.

APPLICATIONS

- Leased line provision
- Metropolitan Area Network Aggregation
- Broadband Digital Loop Carrier
- PON, Cable and WiMax backhaul systems
- Remote concentrator
- Cell Site Backhaul
- Metro Ethernet Equipment
- TDM and LAN aggregation

BLOCK DIAGRAM



GENERAL FEATURES

- ❑ PDH and SONET/SDH Circuit Emulation and Packet Pseudowire Services compliant with MEF standards, IETF draft standards, ITU-T standards, ATM Forum such as RFC4842, MEF 3, MEF 5, MEF 8, ITU-T Y.1413, draft-ietf-pwe3-cesopn, draft-ietf-pwe3-tdmoip-06, ATM Forum af-vtoa-0078.00 1997, etc.
- ❑ Flexible PSN including Ethernet, MPLS, UDP/IP and L2TPv3/IP.
- ❑ Rich of Circuit Emulation modes including SAToP, CESoPSN and TDMoIP
- ❑ Rich of Packet Pseudowire Service mode including ATM/FR/HDLC/Ethernet
- ❑ Supports ATM/FR/HDLC interfaces including SPI-3 and V.35/HSSI
- ❑ Provide IMA pre-processing for ATM Pseudowire
- ❑ Flexible timing mode for TDM service including Differential/Adaptive Clock Recovery, Common Clock, External Clock and Loop-Timing Modes
- ❑ Supports unstructured on-chip and structured utilizing the DS1/E1 and DS3/E3 framers, DS0 XC and CAS processor plus SONET mapping on the Arrive's MSADM, EoPDH and Channelized mapper devices
- ❑ High Pseudowire channels over Ethernet, MPLS or IP packet networks
- ❑ Processing high bi-directional 64 Kbps (DS0) channels from DS1/E1 or from synchronous buses at TDM side
- ❑ Rich of TDM interfaces on the circuit side including MVIP, H-MVIP, ST-Bus, AT PDH Bus, AT VT Expansion Bus, serial DS3/E3/DS1/E1 interfaces, parallel SONET/SDH interfaces
- ❑ Rich of Interfaces on the packet side including an SPI-3, GE RGMII and FE/10/100 interfaces with on-chip MACs
- ❑ Provide pre-processing ability at service side before Pseudowire processing including SONET/SDH framer, PDH framer, PDH monitor, M13/E13, HDLC/ATM encapsulation and IMA
- ❑ Provide one DDR2 SDRAM Interface for Jitter and Queuing buffers
- ❑ Provide synchronous generic 32 bit CPU interface
- ❑ Optionally Provide DMA for OAM packets
- ❑ Implemented in Altera FPGA for easy upgrade and integration with a short time-to-market for new and changes in packet protocol standards
- ❑ Package TBD
- ❑ Power consumption TBD
- ❑ Altera device TBD

FEATURE SUMMARY

Pseudowire Service modes

- ❑ The Thalassa provides rich of Packet Switch Networks (PSN) for Pseudowire application including Ethernet, MPLS, UDP/IP and L2TPv3/IP protocols
- ❑ The Thalassa provides rich of modes for Pseudowire payload encapsulation
- ❑ SAToP mode for DS3/E3/DS1/E1 lines (Structure-Agnostic TDM over Packet) with/without Octect-aligned mode for DS1 CES
- ❑ Structured-Aware mode for structured E1/T1 with/without CAS,
- ❑ NxDS0 mode for structured mode with/without CAS
- ❑ Provide both AAL1 and AAL2 modes for TDM over PSN
- ❑ TDM CEP encapsulation mode for SONET/SDH over PSN compliance with RFC4842
- ❑ ATM over PSN with modes: AALO, AAL5, ATM cell concatenation, etc in both of N to one mode and one to one mode
- ❑ Ethernet over PSN in both raw mode and tagged modes
- ❑ HDLC/PPP over PSN in port mode with optional stripping flags, FCS fields and optionally performing bit/byte stuffing, etc
- ❑ FR over PSN in both port mode and one to one mode with optionally stripping flags, FCS fields and optionally performing bit/byte stuffing, etc

Packet Features

- ❑ Two interfaces at Packet Network side: Ethernet interfaces (GE/FE) and SPI-3 at packet side
- ❑ Redundant modes for GE RGMII interfaces,
- ❑ SMII or SS-SMII10/100 FE interfaces
- ❑ SPI-3 packet interface to NPU, Arrive Titan, Ethernet MACs or other packet processors
- ❑ Four classes of service queues at Transmit packet side with rich of priority mechanisms for QoS function
- ❑ Multiple layers for classification mechanism of incoming packet including 2, 3 and 4 layers to identify destination of packets (TDM, LAN, Host) and their contexts
- ❑ Capacity of Packet re-ordering and system impairment mechanism
- ❑ Capacity of detecting loss of packet, packet mis-ordering, packet delay violation
- ❑ Provide MPLS/Ethernet/IP/ATM OAM extraction and insertion

Ethernet MAC Features

- ❑ Ethernet port with full compliant with 802.3, half/full duplex,
- ❑ VLAN tagging and labeling according to 802.1 P&Q including VLAN staking,
- ❑ Complies with MAC for Gigabit and Fast Ethernet framing, flow control handling and auto-negotiation,
- ❑ Rate limiting based Rx Ethernet FIFO,
- ❑ Jumbo frame capability in Packet Pseudowire application
- ❑ MAC Counters for Ethernet Statistics,
- ❑ Optional FCS Insertion at Transmit Ethernet MAC
- ❑ Supports Ethernet OAM extraction and insertion

Service side and Pre-Processing Features

- ❑ Provide rich of interfaces at Service side
- ❑ Serial DS3/E3/DS1/E1 S1/E1 Interfaces with/without encoder/decoder optionally on per line basic
- ❑ Arrive's PDH bus to carry DS3/E3/DS1/E1 from LIU or framer chip for un-structured mode
- ❑ Arrive's expansion bus, a channelized bus, to carry DS0, DS1/E1 synchronous mapping for structured mode
- ❑ Serial channelized buses, each can be programmed to be one of H.110 CT, MVIP, H-MVIP and ST-Bus , with programmable rates including 2/8/16MHz to carry DS0 for structured mode
- ❑ Parallel SONET/SDH interfaces
- ❑ A SPI-3 interface to carry ATM/HDLC/PPP/FR/Ethernet packet traffic
- ❑ SONET/SDH pre-processing functions for SONET/SDH over PSN
- ❑ DS3/E3/DS1/E1 framers for Structured-Aware mode
- ❑ DS3/E3/DS1/E1 frame monitor for Structured-Agnostic mode
- ❑ M13/E13 function for DS1/E1 multiplexing into DS3/E3
- ❑ ATM/HDLC/PPP/FR/Ethernet encapsulation for serial packet interfaces (HSSI/V.35) carrying serial ATM/HDLC/PPP/FR/Ethernet packet traffic
- ❑ IMA functions for multiplexing ATM physical into one ATM path
- ❑ BERT engines and loopback detection for DS_n channels
- ❑ On-chip TDM performance monitoring including LOS.

Timing and Clock Recovery Features

- ❑ Provide rich of timing mode for each DS_n/En line, each TDM channelized bus: Loop-timing mode, Packet timing mode, External timing mode and Internal timing mode
- ❑ Loop-timing mode: timing is extracted from Rx side of the corresponding line
- ❑ Packet timing: timing is extracted from Ethernet lines or from arriving packets with both adaptive and differential modes with RTP using Built-in DLL separately for each DS_n/En line, each TDM channelized bus with 4 operational modes: locking, hold-over, free-run and power-down modes
- ❑ External timing with primary and secondary source clocks
- ❑ Internal timing: timing is from free-running oscillator or an DLL in hold-over mode
- ❑ Provide jitter buffer to compensate the variation delay of arriving packets meeting with performance of IP/MPLS/Ethernet network
- ❑ Ability of programming the size of the jitter buffer to optimizing the delay of each CES connection in order to meet its TDM latency requirement and optimizing using the external DDR2 SDRAM.

Diagnostic

- ❑ Rich of loopback modes for diagnostic
- ❑ Line loopback in/out for TDM interfaces
- ❑ TDM packet loop out for CES connections: TDM data after being encapsulated is loopback out to decapsulation part
- ❑ Loopback in/out at SPI-3 interface
- ❑ Loopback out at Ethernet interfaces
- ❑ Loopback out received packets after classifying

SPI-3 Features

- Provide one SPI-3 bus with clock rate from 52M to 104M with one of two modes: PHY and Link mode.
- 8/16 logical ports
- Optional provisioning Pre-pended Tag for carrying additional channel IDs and
- Optional providing status bus for physical queue visibility to handle flow control including full, satisfied, hungry and starving statuses

Thalassa Variations

| | | AT6620 | AT6552 | AT6330 |
|---------------------------|---------------------------|---|--|---|
| | Feature | Small PDH TDM and Packet/Cell Pseudowire Emulation over PSN | High PDH TDM and Packet/Cell Pseudowire Emulation over PSN | CEP SONET/SDH Pseudowire Emulation over PSN |
| | FPGA Family | Altera Cyclone | Altera | Altera |
| Capacity | Maximum Throughput | 311M | 2G | 622M |
| | Channel | 256 | 1024 | 336 |
| | DS0 | 2016 | 8192/16384 | -- |
| PSN | Ethernet/MPLS/IP | Yes | Yes | Yes |
| Circuits | DS3/E3/DS1/E1 SAToP | Yes | Yes | -- |
| | DS1/E1 CESoPSN/TDMoIP | Yes | Yes | -- |
| | NxDS0 CESoPSN/TDMoIP | Yes | Yes | -- |
| | STS-1 | -- | -- | Yes |
| | VT/TU | -- | -- | Yes |
| | ATM | Yes | Yes | -- |
| | HDLC | Yes | Yes | -- |
| | PPP | Yes | Yes | -- |
| | FR | Yes | Yes | -- |
| Ethernet | Yes | Yes | -- | |
| Circuit Interface | Serial DS3/E3 | Optional | Optional | -- |
| | Serial DS1/E1 | Optional | Optional | -- |
| | AT PDH Bus | Yes | Optional | -- |
| | AT DS0 Bus | Optional | Optional | -- |
| | H.110/H-MVIP/ST-Bus | Optional | Optional | -- |
| | HSSI | Optional | Optional | -- |
| | V.35 | Optional | Optional | -- |
| | SPI-3 | Optional | Optional | -- |
| OC-N/STM-N | None | -- | OC-12/STM-4 | |
| Packet Interface | Parallel GMII (GE) | 2 | 2 | 1 |
| | Serial MII (FE) | 4 | 8 | 8 |
| | SPI-3 | Optional | 1 | 1 |
| Optional Functions | PDH Framer | Optional | Yes | -- |
| | ATM/HDLC Encapsulation | Optional | Yes | -- |
| | IMA | Optional | Optional | -- |
| RAM | | DDR2 | DDR2 | DDR2 |

Implementation Overview

The Thalassa platform is targeted for FPGA implementation which offers both a fast time to market and flexibility due to the various IETF, MEF, ITU, MFA and IEEE standards still being in flux. Thalassa can be thought of as a menu of user selectable IP which can be integrated into a solution depending on exact customer requirements. Arrive will then assemble and verify the design at both the simulation and hardware level prior to customer delivery thus eliminating issues such as timing closure and at speed performance uncertainty. This FPGA based model offers customers an unbeatable 'custom' solution path that can deliver a low risk solution in the shortest possible time frame, freeing up precious resources to get a jump start on pushing the end product to market. Additionally, depending on end customer price targets there are a number of possible paths to mapping the FPGA to dedicated silicon technologies such as hard copy FPGA, structured ASIC's. These opportunities can be explored by contacting Arrive sales representatives.

The Thalassa platform is intended to apply to high capacity aggregation and gateway applications where a large number and the type of Pseudowires may be structure agnostic or structure aware circuits of TDM PDH services such as nxDS0, DS1/E1, DS3/E3 or a packet/cell service emulation of ATM, Frame Relay, HDLC/PPP, or Ethernet. Thalassa has I/O options that allow virtually any Pseudowire signal source to be easily interfaced to the Thalassa irrespective of how the service arrives (as a native PDH signal or packet service or one from any valid SONET/SDH mapping). In order to support all the valid SONET/SDH mappings for all the possible service payloads, the Thalassa can be seamlessly with the Arrive Elara AT4848 family and Europa AT2450 products which offer outstanding mapping capabilities. Thalassa may also be interfaced with most third party DS0 devices for nxDS0 services through the St-Bus, H.110, H-MVIP, AT-EXP, SPI-3 buses or ATM IMA and FR/PPP Multi-link devices through its SPI-3 service side packet bus.

Thalassa Applications Diagram

