

GENERAL DESCRIPTION

TDM networks have largely dominated in the world for many decades, and these legacy networks cannot suddenly be replaced by efficient and very-scalable PSNs (packet switched networks). Pseudowire technology is generally regarded as one of the best ways to make the transition from TDM networks to packet switched networks smoothly and economically without significant service down time. PWE (Pseudowire Emulation) technology allows the continued use of legacy equipment while transitioning to PSN equipment. When properly implemented, users of legacy equipment should be able to transition from legacy networks to PSN, and continue to offer the same characteristics and performance as the native legacy networks.

Meanwhile, advances to 3G -and beyond- mobile services create demands for ever increasing bandwidth. At the same time, mobile providers are continually seeking ways to lower the cost of traffic backhaul. For these reasons, pseudowire technology is becoming a preferred method.

The Arrive Technologies Thalassa is a family of Complete Pseudowire and Mobile Backhaul System-on-a-Chip devices for those purposes. Thalassa provides a total solution for all areas: first-mile equipment with 4, 8 or up to 32 DS1/E1 lines; aggregation nodes with up to 84/63 DS1/E1 lines; or high-density aggregation nodes or Radio Network Controllers (RNC) and edge transport nodes with 336/252 DS1/E1 lines or up to 672/504 DS1/E1 lines. The Thalassa family offers equipment makers a single chip solution. PCB size, BOM, and power consumption are reduced dramatically by a single chip solution.

The AT6012 is a member of Thalassa family. AT6012 provides one STS-12/STM-4 bandwidth for complete pseudowire protocols, such as SAToP, CESoPSN, MEF-8, CEP, ATM pseudowires (PW), PPP PW, HDLC PW, Ethernet PW. The AT6012 also provides another STS-12/STM-4 bandwidth concatenated for ATM stream to ATM switch/aggregation and dedicated ATM pseudowire. All legacy protocols: DS0, DS1, E1, DS3, E3, SONET/SDH, ATM, IMA, HDLC, PPP, FR, MLPPP, Ethernet may be tunneled concurrently within 1024 PW connections over PSN networks. The AT6012 integrates OC-12/STM-4, OC-3/STM-4 for SONET/SDH ports carrying high channel DS1/E1 lines, a programmable hybrid buses for DS1/E1/DS3/E3 ports and Gigabit Ethernet ports for PSN side. AT6012 can connect to many kinds of PSN networks: IPv4, IPv6, MPLS, and Ethernet.

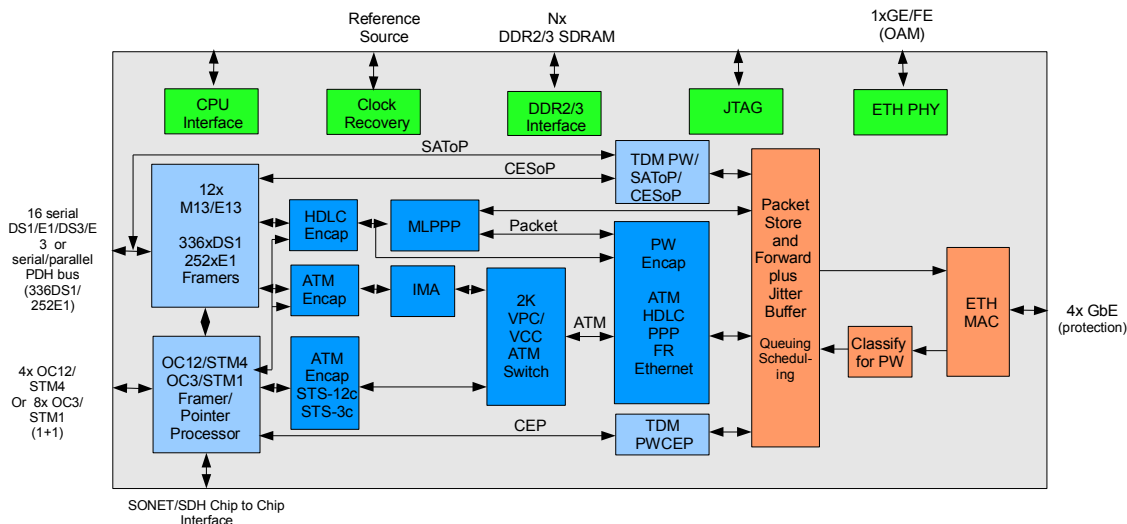
KEY FEATURES

- ❑ A complete Pseudowire Processor, with a single software kit allowing development of products in applications ranging from the-first-mile to aggregation
- ❑ Pseudowire support for DS1, E1, DS3, E3, SONET/SDH, ATM, HDLC, PPP, FR, and Ethernet over PSN
- ❑ High throughput
 - 1xSTS-12/STM-4 bandwidth channelized for complete pseudowire protocols
 - 1xSTS-12/STM-4 bandwidth concatenated for ATM stream to ATM switch/aggregation and dedicated ATM pseudowire
 - 1024 PW connections
- ❑ Support for various legacy interfaces, both electrical and optical: DS1, E1, DS3, E3 and SONET/SDH
- ❑ Pseudowire solutions for mobile backhaul applications based on TDM, IMA, MLPPP and Ethernet
- ❑ Clock recovery algorithm from PSN to meet ITU G.8261 and MEF22
- ❑ Programmable hybrid buses, shared-pin for
 - 16 serial interfaces directly to LIU devices for DS1/E1, up to 12 serial interfaces for DS3/E3
 - 21 serial interfaces for star connection to a LIU linecard with multiple DS1/E1, each for carrying up to 16 DS1/E1
 - One programmable 8-bit SONET/SDH bus with/without frame synch signals
- ❑ Four serial interfaces for OC-3/STM-1 and Four multi-rate serial interface for OC-12/STM-4/OC-3/STM-1 without or with port protection, each with internal SerDes option.
- ❑ Four serial interfaces/SGMII for GbE with protection, two interfaces without protection, with internal SerDes option
- ❑ One SGMII for GbE for carrying OAM packets
- ❑ Very low-cost DDR2/3 SDRAM for large buffers
- ❑ Provided as an upgradeable device (FPGA) bitstream, or as a hardwired device, allowing options for upgradeable features or lower device cost

APPLICATIONS

- ❑ Gateway of Pseudowire and Voice Trunking
- ❑ Aggregation of Packet Mobile Backhaul

AT6012 BLOCK DIAGRAM



FEATURES SUMMARY

Interworking

- ❑ DS1/E1/DS3/E3 ↔ SAToP/CESoPSN/MEF8 ↔ Ethernet/MPLS/IPv4/IPv6 ↔ GbE/FE
- ❑ DS3/E3 ↔ DS1/E1 ↔ SAToP/CESoPSN/MEF8 ↔ Ethernet/MPLS/IPv4/IPv6 ↔ GbE/FE
- ❑ SONET/SDH ↔ DS1/E1/DS3/E3 ↔ SAToP/CESoPSN/MEF8 ↔ Ethernet/MPLS/IPv4/IPv6 ↔ GbE/FE
- ❑ SONET/SDH ↔ VC11/VC12/VC3/VC4 ↔ CEP ↔ Ethernet/MPLS/IPv4/IPv6 ↔ GbE/FE
- ❑ DS1/E1 ↔ ATM ↔ IMA ↔ ATM PW ↔ Ethernet/MPLS/IPv4/IPv6 ↔ GbE/FE
- ❑ SONET/SDH ↔ VC11/VC12/VC3/VC4 ↔ ATM ↔ IMA ↔ ATM PW ↔ Ethernet/MPLS/IPv4/IPv6 ↔ GbE/FE
- ❑ SONET/SDH ↔ DS1/E1 ↔ ATM ↔ IMA ↔ ATM PW ↔ Ethernet/MPLS/IPv4/IPv6 ↔ GbE/FE
- ❑ DS1/E1 ↔ HDLC/PPP ↔ HDLC/PPP PW ↔ Ethernet/MPLS/IPv4/IPv6 ↔ GbE/FE
- ❑ SONET/SDH ↔ VC11/VC12 ↔ HDLC/PPP ↔ HDLC/PPP PW ↔ Ethernet/MPLS/IPv4/IPv6 ↔ GbE/FE
- ❑ SONET/SDH ↔ DS1/E1 ↔ HDLC/PPP ↔ HDLC/PPP PW ↔ Ethernet/MPLS/IPv4/IPv6 ↔ GbE/FE
- ❑ DS1/E1 ↔ HDLC/PPP ↔ MLPPP ↔ IPv4/IPv6/Ethernet PW ↔ Ethernet/MPLS/IPv4/IPv6 ↔ GbE/FE
- ❑ SONET/SDH ↔ VC11/VC12/VC3/VC4 ↔ HDLC/PPP ↔ IPv4/IPv6/Ethernet PW ↔ Ethernet/MPLS/IPv4/IPv6 ↔ GbE/FE
- ❑ SONET/SDH ↔ DS1/E1 ↔ HDLC/PPP ↔ MLPPP ↔ IPv4/IPv6/Ethernet PW ↔ Ethernet/MPLS/IPv4/IPv6 ↔ GbE/FE
- ❑ SONET/SDH ↔ DS1/E1/DS3/E3
- ❑ SONET/SDH ↔ DS1/E1 ↔ DS3/E3
- ❑ DS1/E1 ↔ ATM ↔ IMA ↔ ATM Switch ↔ ATM ↔ VC11/VC12/VC3/VC4 ↔ SONET/SDH
- ❑ DS1/E1 ↔ ATM ↔ IMA ↔ ATM Switch ↔ IMA ↔ ATM ↔ VC11/VC12 ↔ SONET/SDH

TDM over PSN

- ❑ Up to 12 DS3/E3, 336DS1/252E1, 8064 DS0
- ❑ Up to 1024 pseudowire connections
- ❑ SAToP according to RFC4553, Y.1413, Y.1453, MFA 8.0, MEF8 with and without octet-aligned mode
- ❑ CESoPSN according to RFC5086, Y.1413, Y.1453, MFA 8.0, MEF8 with and without CAS and fragmentation
- ❑ Support RTP header
- ❑ Jitter buffer for PDV (packet delay variation) tolerance, packet re-ordering and clock recovery from PSN
- ❑ Programmable size up to 256ms of jitter buffer to optimize delay of each connection in order to meet standard requirements

Timing and Clock Recovery from PSN

- ❑ Support ACR (Adaptive Clock Recovery) and DCR (Differential Clock Recovery) to meet jitter and wander requirements G.8261, G.823 and G.824
- ❑ Individual built-in DPLL for each of DS1/E1/DS3/E3 for clock recovery from PSN with locking, hold-over, free-run and power-down modes
- ❑ Rich set of timing modes for DS3/E3/DS1/E1: packet timing, external timing, internal timing and loop timing
- ❑ Clock frequency generation meets 16ppb requirements
- ❑ Accept packet stream with offsets from 100pps to 8000pps
- ❑ External PRC (Primary Reference Clock) reference input for DCR mode

SONET/SDH over PSN

- ❑ Support VC11,VC12,VC3,VC4 according to RFC4842
- ❑ Support two modes of SONET/SDH pointer management: Explicit Pointer Adjustment Relay (EPAR) and Adaptive Pointer Management (APM)
- ❑ Support Dynamic Bandwidth Allocation (DBA): suppression of the SPE/VT transmission when AIS-P/V or SPE/VT unequipped

ATM over PSN

- ❑ ATM pseudowire encapsulation according to RFC4717
- ❑ Up to 1024 pseudowire connections
- ❑ ATM One-to-One, ATM N-to-One, AAL5-SDU frame
- ❑ Integrate ATM switching capability
- ❑ Independent buffer for PDV tolerance, packet re-ordering from PSN

HDLC/PPP/FR/Ethernet over PSN

- ❑ HDLC pseudowire encapsulation according to RFC4618
- ❑ Up to 336 pseudowire connections
- ❑ Provide port mode for HDLC/PPP/FR PW
- ❑ Provide raw mode for Ethernet PW
- ❑ Removal of FCS, Flag optionally on a per-connection basis
- ❑ Perform bit/byte stuffing optionally on a per-connection basis
- ❑ Independent buffer for delay tolerance, packet re-ordering from PSN

PDH Features

- ❑ 336 DS1/J1 framers, 252 E1 framers, 12 DS3/E3 framers
- ❑ DS1 framing: SF/ESF/SLC-96/DDS, J1 framing: SF/ESF, E1 framing: CRC-4 and non-CRC-4, E3 framing: ITU-T G.751 or G.832, DS3 framing: C-bit parity or M23 framing
- ❑ Support M13/E13 multiplexers with DS3/E3 framers
- ❑ Bit asynchronous or byte synchronous mapping of DS1/J1 to VT1.5/TU11 or E1 to VT2/TU12
- ❑ Support mapping of VT1.5/VT2/TU11/TU12 and DS3/E3 to SONET/SDH SPE
- ❑ Jitter attenuation for DS1/E1 to DS3/E3 Mux, Asynchronous DS1/E1 to VT/TU Map, Asynchronous DS3/E3 to STS1/VC3 Map
- ❑ Alarm detection and processing: AIS, RDI, RAI, LOS, OOF, LOF, LOMF, FERF
- ❑ Counters: CRC error, FEBE, BIP-8
- ❑ Support FDL (facility data link), BOC (Bit Oriented Commands)
- ❑ Loopback code detection and insertion
- ❑ Loopback data path: local, remote, line signal, payload
- ❑ BERT detection and insertion

SONET/SDH Features

- ❑ Independently-programmable interfaces for 4x OC-3/STM-1 and 4x OC-12/STM-4/OC-3/STM-1 with loop-time capability
- ❑ High order and low order pointer processing
- ❑ Support high order contiguous concatenation
- ❑ Full SONET/SDH section/line overhead processing
- ❑ Full STS/VC and VT/TU path monitoring/termination
- ❑ Hardware-based BER detection
- ❑ Support DCC extraction and insertion for CPU processing

Data Encapsulation

- ❑ ATM, PPP/HDLC/ LAPS simultaneously, full duplex being carried by DS1/E1, framed, unframed, fractional, NxDS0, VT1.5/VC11, VT2/VC12, VC3, VC4
- ❑ Up to 336 data channels
- ❑ Cell HEC and packet FCS checker/generator and 1-bit HEC error correction
- ❑ Idle/unassigned cell and aborted sequence detection/ generation
- ❑ Cell/packet payload scrambling/de-scrambling
- ❑ Bit stuffing and byte stuffing for HDLC/PPP/LAPS
- ❑ Support 16 or 32 bit frame check sequence field (FCS) per channel data
- ❑ Extraction and insertion header field support

FEATURES SUMMARY (Cont'd)**Inverse Multiplexing for ATM (IMA)**

- ❑ Support ATM Forum Inverse Multiplexing for ATM Specification Version 1.0 (symmetrical mode) and 1.1
- ❑ Up to 336 links from DS1, E1, VT1.5/VC11, VT2/VC12
- ❑ Up to 168 IMA groups, each group can support 1 to 32 links
- ❑ Up to 256ms delay compensation for the IMA links
- ❑ Group and Link state machine implemented by hardware
- ❑ ITC/CTC stuffing mode
- ❑ IMA frame length: 32, 64, 128, or 256
- ❑ Support for all symmetrical/asymmetrical modes
- ❑ Group and link performance counters

Multi-link PPP (MLPPP)

- ❑ Provide MLPPP as per RFC1990 with extension to LCP option
- ❑ Up to 336 links
- ❑ Up to 168 bundles, each bundle can support 1 to 16 links
- ❑ Up to 100ms delay compensation for the MLPPP links
- ❑ Provide packet fragmentation or full packet
- ❑ Support multi-class according to RFC2686, up to 16 class
- ❑ Provide insertion and extraction of LCP frame as RFC1661
- ❑ Max MRU of 1543 bytes (corresponds to 1536-byte frames)
- ❑ Support Short/Long sequence number
- ❑ Provide BCP as RFC3518
- ❑ Loop detection on the LCP level
- ❑ Bundle and link performance counters

ATM Switching and Policing

- ❑ Up to 2048 VP and VC connections with full UNI/NNI VP and VC ranges
- ❑ Switching based on VPI, VCI, the interface ID and the interface type (UNI or NNI)
- ❑ Support Virtual Channel Identifier and Virtual Path Identifier (VPI/VCI) translation
- ❑ Up to 2048 policing profiles for 2048 virtual connections
- ❑ Up to 2048 virtual connections shaping
- ❑ Support 4 traffic classes (CBR, VBR, UBR and UBR+) with strict priority mode per ports
- ❑ Support rate limit for OC-12/STM-4/OC-3/STM-1 port interface

Quality of Service over PSN

- ❑ Support QoS for Layer-2 network, MPLS networks and IP networks: VLAN priority bits, EXP bits, TOS or DSCP bits
- ❑ 4 classes of services (4 queues) for each of the PSN interfaces
- ❑ Provide DWRR (Deficit Weighted Round Robin) and FP (Fixed Priority) scheduling algorithms

PSN Protocols

- ❑ Support MPLS, MPLS over IP, MPLS over GRE, MPLS with/without PHP
- ❑ Support UDP/IPv4, UDP/IPv6
- ❑ Support MEF
- ❑ Support L2TPv3/IPv4, L2TPv3/IPv6
- ❑ Support VLAN, Q-in-Q

Ethernet Features

- ❑ 4x Gigabit Ethernet interface in compliant with IEEE 802.3
- ❑ Programmable preamble size, erroneous preamble detection
- ❑ Provide flow control protocol
- ❑ Support jumbo frame for EoS and EoPDH
- ❑ MAC Counters for Ethernet Statistics
- ❑ Support Ethernet rate limitation

OAM and Diagnostics

- ❑ Ethernet
 - Supports EFM OAM IEEE 802.3ah processing
- ❑ MPLS
 - Supports packet insertion and extraction to CPU for LDP (RFC4447), LSP-Ping
- ❑ IP
 - Support packet insertion and extraction via CPU for ARP, ICMP
- ❑ Pseudowire
 - Support pseudowire OAM message mapping (draft-ietf-pwe3-oam-msg-map-10)
 - Support frame insertion and extraction to CPU for VCCV (RFC5085), VCCV-BFD (draft-ietf-pwe3-vccv-bfd-04)
- ❑ ATM
 - Support fault management (F4/F5 AIS, RDI, Continuity Check and Loopback) processing, for VP/VC, Segment/End-to-end flows on all VCs in compliance with I.610
 - Support cell test towards the ATM ports
 - Support alarm forwarding between of ATM ports and PSN ports
- ❑ In-band system management channel:
 - Support packet insertion and extraction to CPU: IP, Pseudowire connection, VLAN and ATM VP/VC
- ❑ Support loopbacks:
 - Parallel loopbacks on SONET/SDH ports
 - Remote loopback on Ethernet ports
 - Remote loopback on per Pseudowire
 - In-band loopbacks on DS1,E1,DS3,E3
 - ATM VC/VP loopbacks

Clock Synchronization

- ❑ Clock selection from interface-based synchronization (SONET/ SDH, DS1, E1, Synchronous Ethernet), recovered clock from PSN for external timing device.
- ❑ Distribute the master clock to remote PSN peers using timing packets with dedicated PWs (Uni-cast) or a single multi-cast IP
 - Packet format: SAToP
 - Programmable packet rate

Protection and Redundancy

- ❑ Provide Ethernet port protection facilities: 1:1, link aggregation IEEE 802.3ad
- ❑ Provide SONET/SDH protection facilities: 1+1/APS,chip-to-chip
- ❑ Provide pseudowire protection facilities by using pseudowire connectivity check – VCCV-BFD according to draft-ietf-pwe3-vccv-bfd-04

CPU, RAM and Device Technology

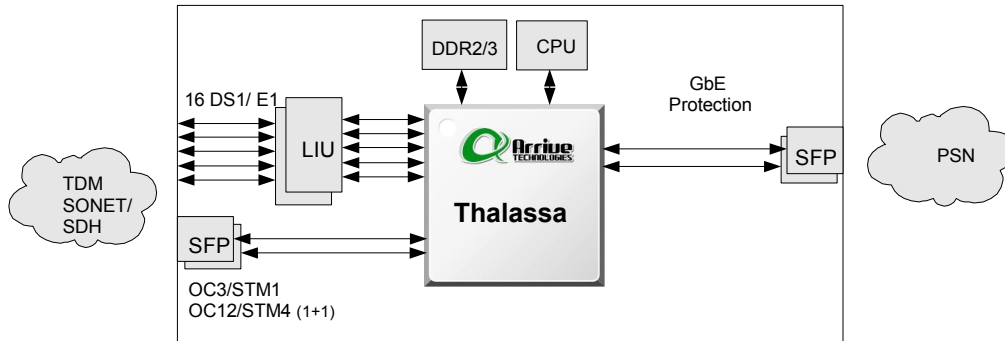
- ❑ Generic 32-bit CPU interface
- ❑ Low-cost DDR2/3-SDRAM for external memory

High level Software Driver

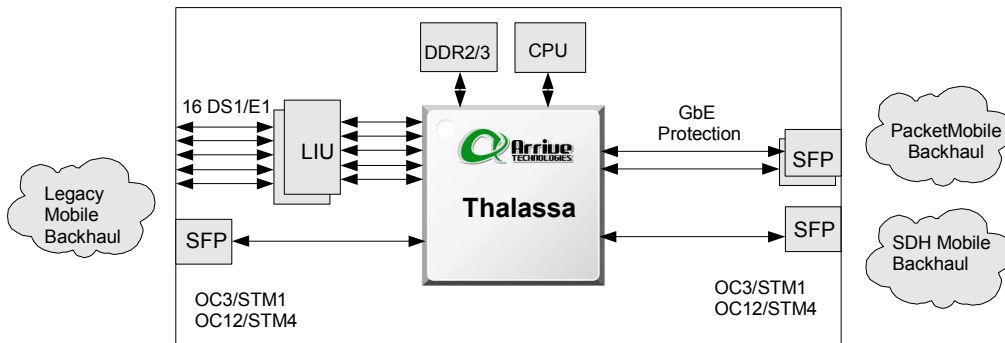
- ❑ One API software driver for the whole family of devices
- ❑ High-level API software driver architecture approach
- ❑ Platform independent and Operating System (OS) independent
- ❑ Compliant to ANSI-C

APPLICATION SAMPLES

Pizza-box, TDM/ATM/HDLC/PPP/Ethernet pseudowires



Pizza-box, Hybrid backhaul for HSDPA



Linecard, up to 336 DS1/ 252 E1 transported by 4 OC3/STM1, GbE backplane

