

### GENERAL DESCRIPTION

TDM networks have largely dominated in the world for many decades, and these legacy networks cannot suddenly be replaced by efficient and very-scalable PSNs (packet switched networks). Pseudowire technology is generally regarded as one of the best ways to make the transition from TDM networks to packet switched networks smoothly and economically without significant service down time. PWE (Pseudowire Emulation) technology allows the continued use of legacy equipment while transitioning to PSN equipment. When properly implemented, users of legacy equipment should be able to transition from legacy networks to PSN, and continue to offer the same characteristics and performance as the native legacy networks.

Meanwhile, advances to 3G, 4G, LTE -and beyond- mobile services create demands for ever increasing bandwidth. At the same time, mobile providers are continually seeking ways to lower the cost of traffic backhaul. For these reasons, pseudowire technology is becoming a preferred method.

The Arrive Technologies Thalassa is a family of Complete Pseudowire and Mobile Backhaul System-on-a-Chip devices for those purposes. Thalassa provides a total solution for all areas: first-mile equipment with 1, 4, 8 or up to 32 DS1/E1/J1 lines; aggregation nodes with up to 84/63 DS1/E1 lines; or high-density aggregation nodes or Radio Network Controllers (RNC) and edge transport nodes with 336/252 DS1/E1 lines or up to 672/504 DS1/E1 lines. The Thalassa family offers equipment makers a single chip solution. PCB size, BOM, and power consumption are reduced dramatically by a single chip solution.

The AF6xxx devices are FPGA-based, low-channel-count members of the Thalassa family. AF6xxx devices provides up to 32 DS1/E1 bandwidth for complete pseudowire protocols, such as SAToP, CESoPSN, MEF-8, ATM pseudowires (PW). All legacy protocols: DS0, DS1, E1, ATM, and IMA may be tunneled concurrently within 128 PW connections over PSN networks. AF6xxx devices can connect to many kinds of PSN networks: IPv4, IPv6, MPLS, and Ethernet.

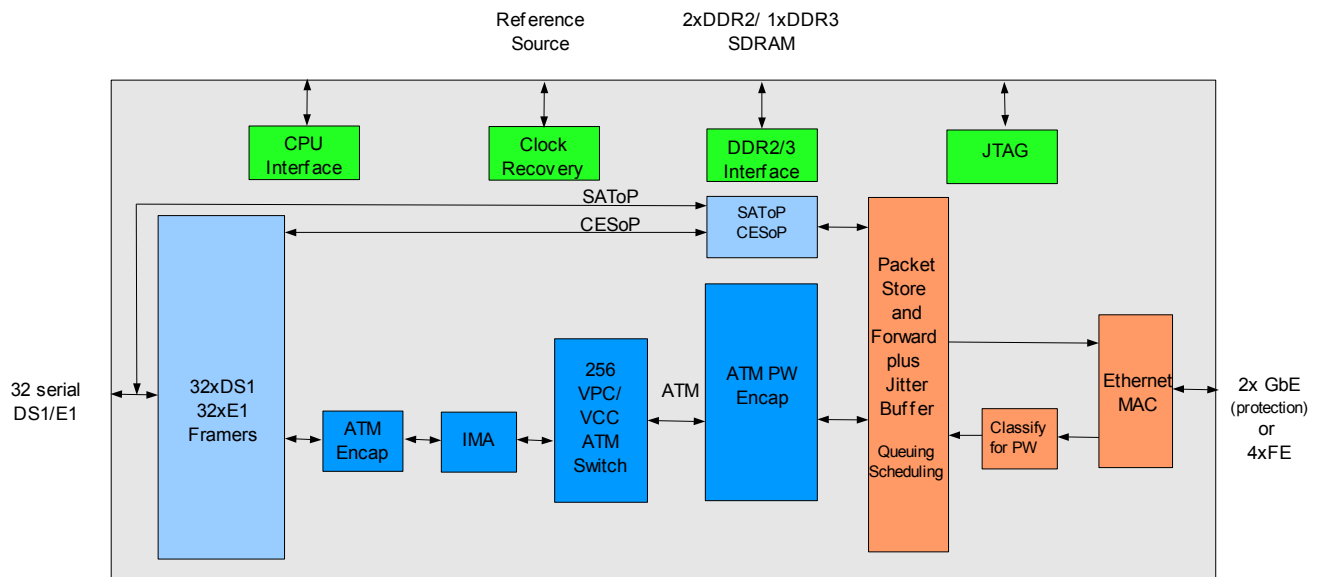
### KEY FEATURES

- ❑ A low-cost, FPGA-based Pseudowire Processor with a single software kit
- ❑ SAToP/CESoPSN and ATM Pseudowire support for up to 32 DS1/E1 over PSN
- ❑ 2 GE (SGMII) or 4 FE (SMII) with protection at Packet Switch Network Interface
- ❑ Low-cost DDR2/3 SDRAM for packet buffer
- ❑ Up to 128 Pseudowire connections
- ❑ Up to 32 DS1/E1 framers (also supports Japanese J1 mode)
- ❑ Clock recovery algorithm from PSN meeting ITU G.8261 and MEF22 recommendations
- ❑ Generic 16-bit CPU interface
- ❑ Available on low-cost FPGA supplied by Arrive IP or customer's FPGA

### APPLICATIONS

- ❑ Gateway of Pseudowire and Voice Trunking

### AF6xxx BLOCK DIAGRAM



## FEATURES SUMMARY

### Interworking

- ❑ PDH PW: RFC3985, RFC4553, RFC5086, MEF8, ITU-T Y1413
  - DS1/E1 ↔ SAToP ↔ Ethernet/MPLS/IPv4/IPv6 ↔ GE/FE
  - DS1/E1 ↔ CESoPSN ↔ Ethernet/MPLS/IPv4/IPv6 ↔ GE/FE
- ❑ ATM PW: RFC4717
  - DS1/E1 ↔ ATM ↔ Without IMA ↔ ATM PW ↔ Ethernet/MPLS/IPv4/IPv6 ↔ GE/FE
  - DS1/E1 ↔ ATM ↔ IMA ↔ ATM PW ↔ Ethernet/MPLS/IPv4/IPv6 ↔ GE/FE

### PDH over PSN

- ❑ Up to 32 DS1/E1/J1 direct LIU interfaces
- ❑ Up to 128 pseudowire connections
- ❑ SAToP according to RFC4553, Y.1413, Y.1453, MFA 8.0, MEF8 with and without octet-aligned mode
- ❑ CESoPSN according to RFC5086, Y.1413, Y.1453, MFA 8.0, MEF8 with and without CAS and fragmentation
- ❑ Support RTP header
- ❑ Jitter buffer for PDV (packet delay variation) tolerance, packet re-ordering and clock recovery from PSN
- ❑ Programmable size up to 256ms of jitter buffer to optimize delay of each connection in order to meet standard requirements

### Timing and Clock Recovery from PSN

- ❑ Support ACR (Adaptive Clock Recovery) and DCR (Differential Clock Recovery) to meet jitter and wander requirements in G.8261, G.823 and G.824 recommendations
- ❑ Individual built-in DPLL for each of DS1/E1 for clock recovery from PSN with locking, hold-over, free-run and power-down modes
- ❑ Rich set of timing modes for DS1/E1: packet timing, external timing, internal timing and loop timing
- ❑ Clock frequency generation meets 16ppb requirements
- ❑ Accept timing packet stream with offsets from 100pps to 8000pps
- ❑ External PRC (Primary Reference Clock) reference input for DCR mode

### ATM over PSN

- ❑ ATM pseudowire encapsulation according to RFC4717
- ❑ Up to 128 pseudowire connections
- ❑ ATM One-to-One, ATM N-to-One, AAL5-SDU frame
- ❑ Integrate ATM switching capability
- ❑ Independent buffer for PDV tolerance, packet re-ordering from PSN

### ATM Switching and Policing

- ❑ Up to 256 VP and VC connections with full UNI/NNI VP and VC ranges
- ❑ Switching based on VPI, VCI, the interface ID and the interface type (UNI or NNI)
- ❑ Support Virtual Channel Identifier and Virtual Path Identifier (VPI/VCI) translation
- ❑ Up to 256 policing profiles for 256 virtual connections
- ❑ Up to 256 virtual connections shaping
- ❑ Supports 4 traffic classes (CBR, VBR, UBR and UBR+) with strict priority mode per ports.

### PDH Features

- ❑ 32 DS1/E1/J1 framers
- ❑ DS1 framing: SF/ESF, J1 framing: SF/ESF, E1 framing: CRC-4
- ❑ Alarm detection and processing: AIS, RDI, RAI, LOS, OOF, LOMF, FERF
- ❑ Counters: F-bit error, CRC error, FEBE
- ❑ Support FDL (facility data link), BOC (Bit Oriented Commands)
- ❑ Loopback data path: local, remote, line signal, payload
- ❑ Optional in-band loopcode detection/insertion
- ❑ BERT detection and insertion

### ATM Encapsulation

- ❑ Cell HEC and packet FCS checker/generator and 1-bit HEC error correction
- ❑ Idle/unassigned cell and aborted sequence detection/ generation
- ❑ Cell payload scrambling/de-scrambling
- ❑ Extraction and insertion header field support

### Inverse Multiplexing for ATM (IMA)

- ❑ Support ATM Forum Inverse Multiplexing for ATM Specification Version 1.0 (symmetrical mode) and version 1.1
- ❑ Up to 32 links from DS1, E1, J1
- ❑ Up to 16 IMA groups, each group can support from 1 to 32 links
- ❑ Up to 256ms delay compensation for the IMA links
- ❑ Group and Link state machine implemented by hardware
- ❑ ITC/CTC stuffing mode
- ❑ IMA frame length: 32, 64, 128, or 256
- ❑ Support for all symmetrical/asymmetrical modes
- ❑ Group and link performance counters

### Quality of Service over PSN

- ❑ Supports QoS for Layer-2 network, MPLS networks and IP networks: VLAN priority bits, EXP bits, TOS or DSCP bits
- ❑ 4 classes of services (4 queues) for each of the PSN interfaces
- ❑ Provides DWRR (Deficit Weighted Round Robin) and FP (Fixed Priority) scheduling algorithms

### PSN Protocols

- ❑ Supports MPLS, MPLS over IP, MPLS over GRE, MPLS with/without PHP
- ❑ Supports UDP/IPv4, UDP/IPv6
- ❑ Supports MEF
- ❑ Supports L2TPv3/IPv4, L2TPv3/IPv6
- ❑ Supports VLAN, Q-in-Q

## **FEATURES SUMMARY (Cont'd)**

### **Ethernet Features**

- 2x Gigabit Ethernet interfaces or 4x Fast Ethernet interfaces in compliant with IEEE 802.3
- Programmable preamble size, erroneous preamble detection
- Provides flow control protocol
- MAC Counters for Ethernet Statistics
- Supports Ethernet rate limitation

### **OAM and Diagnostics**

- Ethernet
  - Supports packet insertion and extraction to CPU for EFM OAM IEEE 802.3ah processing
- MPLS
  - Supports packet insertion and extraction to CPU for LDP (RFC4447), LSP-Ping
- IP
  - Supports packet insertion and extraction via CPU for ARP, ICMP
- Pseudowire
  - Supports pseudowire OAM message mapping (draft-ietf-pwe3-oam-msg-map-10)
  - Supports frame insertion and extraction to CPU for VCCV (RFC5085), VCCV-BFD (draft-ietf-pwe3-vccv-bfd-04)
- ATM
  - Supports fault management (F4/F5 AIS, RDI, Continuity Check and Loopback) processing, VP/VC, Segment/End-to-end flows on all VCs in compliance with I.610
  - Supports cell test towards ATM ports
  - Supports alarm forwarding between ATM ports and PSN ports

### **Clock Synchronization**

- Provide reference clock output selected from DS1/E1 interfaces or Ethernet interfaces or recovered clock from PSN (ACR/DCR) for external timing device
- Distribute the master clock to remote PSN peers using timing packets with dedicated PWs (Uni-cast) or a single multi-cast IP
  - Packet format: SAToP
  - Programmable packet rate

### **Protection and Redundancy**

- Provides Ethernet port protection facilities: 1:1, Link aggregation IEEE 802.3ad
- Provides pseudowire protection facilities by using pseudowire connectivity check – VCCV-BFD according to draft-ietf-pwe3-vccv-bfd-04

### **CPU, RAM and Device Technology**

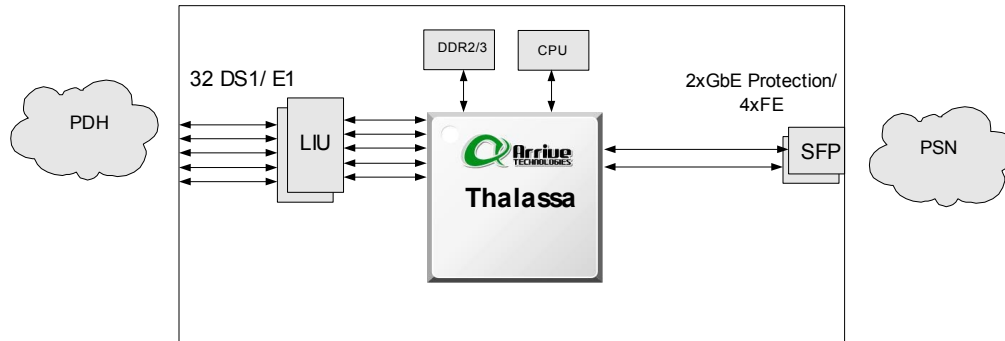
- Generic 16-bit CPU interface
- Low-cost DDR2/3-SDRAM for external memory

### **High level Software Driver**

- One API software driver for the whole family of devices
- High-level API software driver architecture approach
- Platform independent and Operating System (OS) independent
- Compliant to ANSI-C

## APPLICATION SAMPLES

### Pizza-box, TDM/ATM/HDLC/PPP/Ethernet pseudowires



## DERIVATIVES

### Thalassa AF610x and AF620x Family

Name code		AF6201	AF6200	AF6101	AF6100
<b>Feature</b>		128 PDH/ATM/Pkt PW	64 PDH/ATM/Pkt PW	128 PDH PW	64 PDH PW
<b>Application</b>		Router/cell-site gateway	Hub site gateway	CPE, cell-site gateway	CPE, cell-site gateway
<b>Capacity</b>	Throughput	32 DS1/E1	16 DS1/E1	32 DS1/E1	16 DS1/E1
	PW connections	128	64	128	64
<b>PSN</b>	Ethernet/MPLS/IP	Yes	Yes	Yes	Yes
<b>Circuits</b>	PDH PW	Yes	Yes	Yes	Yes
	ATM PW	Yes	Yes	No	No
<b>ATM</b>	IMA/ATM SW	Yes	Yes	No	No
	Max number links	32	16	No	No
	Max number groups	16	8	No	No
	Links/Groups	1 to 32	1 to 16	No	No
	Delay compensation	256 ms	256 ms	No	No
<b>Circuit Interface</b>	Serial DS1/E1	32	16	32	16
	PSN	2xGE(1+1)/4xFE	2xFE	2xGE(1+1)/4xFE	2xFE
	External Memory	2x16-bit DDR2/3	1x16-bit DDR2/3	2x16-bit DDR2/3	1x16-bit DDR2/3
<b>PDH Timing</b>	ACR/DCR/LoopTime/External	Yes	Yes	Yes	Yes
<b>FPGA resource</b>	LE	110KLE	TBD	75KLE	TBD
	Memory	2.3M	TBD	1.5M	TBD

## Thalassa AF6900-x Family

Name code		AF6900-16	AF6900-8	AF6900-4	AF6900-1	AF6900-1S
<b>Feature</b>		16 SAToP PW	8 SAToP PW	4 SAToP PW	1 SAToP PW	1 SAToP PW
<b>Application</b>		Router/cell-site gateway	Hub site gateway	CPE, cell-site gateway	CPE, cell-site gateway	SFP
<b>Capacity</b>	Throughput	16DS1/E1	8DS1/E1	4DS1/E1	1DS1/E1	1DS1/E1
	PW connections	16	8	4	1	1
<b>PSN</b>	Ethernet/MPLS/IP	Yes	Yes	Yes	Yes	Yes
<b>Jitter Buffer</b>		256 ms	256 ms	256 ms	256 ms	200 ms
<b>Circuit Interface</b>	Serial DS1/E1	16	8	4	1	1
	PSN	1xFE	1xFE	1xFE	1xFE	1xFE
	External Memory	1x16-bit DDR2/3	1x16-bit DDR2/3	1x16-bit DDR2/3	1x16-bit DDR2/3	No
	CPU	16-bit	16-bit	16-bit	16-bit	No
<b>PDH Timing</b>	ACR/DCR/ LoopTime/ External	Yes	Yes	Yes	Yes	Yes
<b>FPGA resource</b>	LE	45KLE	35KLE	25KLE	20KLE	15KLE
	Memory	500K	300K	200K	100K	500K