Key Features

- Non-blocking Carrier Ethernet switching with integration of packet processing and traffic management
- Supports MEF E-Line, E-LAN, E-Tree services concurrently
- Supports Synchronous Ethernet network timing
- Ethernet OAM and protection switching
- E1/T1/J1 transported transparently over Carrier Ethernet
- Implemented in low cost FPGA for easy upgrade, integration, feature customization, enhancements and updated packet protocols
- Easy to design as an ASSP device with high level software drivers of Calypso family

General Description

Calypso AF5503-8 is a Carrier Ethernet switch that highly integrates a Packet Processor and Traffic Manager for carrier-class Ethernet networks. It enables carrier grade service providers to leverage MEF E-line, E-LAN, E-Tree services concurrently in compliance with IEEE, IETF, ITU-T, MEF, and MFA standard specifications. Calypso AF5503-8 provides non-blocking switching and incorporates advanced Quality of Service for high reliability Ethernet transport networks.

Calypso AF5503-8 contains three Gigabit Ethernet ports and two 10/100 Mbps Ethernet ports. Gigabit ports integrate CDRs that allow to simply connect to SFP modules.

Calypso AF5503-8 integrates eight E1/T1/J1 ports to transport transparently E1/T1/J1 over Carrier Ethernet networks. These interfaces connect directly to LIU devices without glue logic.

Calypso AF5503-8 can be used on various packet system line cards and pizza-box systems. Calypso is a companion with Arrive's family of pseudowire, mobile backhaul and legacy MSPP and Data mapper devices to provide hybrid TDM/Packet network interworking linecards and systems.

Calypso AF5503-8 is implemented in a Field Programmable Gate Array (FPGA) for easy field upgrades, feature customization, standards updates. The Calypso FPGA approach assures compliance tracking with changes of growing technology standards and allows a very short time-to-market.

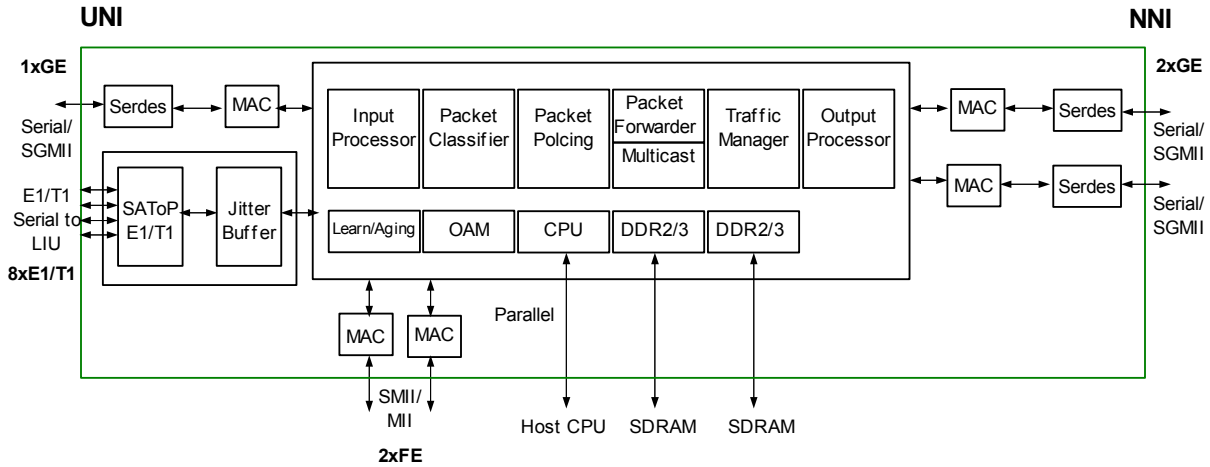
Calypso AF5503-8 is a member of Arrive's Calypso family of Packet Processing, Switch and Flow Processors targeted with different capacities, I/O, features and cost to meet the varied needs of equipment suppliers. Calypso AF5503-8 is fitted in Altera low-cost FPGA families.

In accompanying easy design as an ASSP device, Calypso AF5503-8 software driver is provided as high level to reduce significant Time-to-Market. The software driver is compatible with any member of Calypso family. Calypso evaluation platforms available for demonstration and evaluation. Customers' software development cycles take advantage of the evaluation platform for software and application development prior to system PCB existence.

Applications

- Metro Ethernet Transport
- Packet-based Mobile Wireless Backhaul
- Carrier Ethernet Routers and Switches

Block Diagram



Feature Summary

Interface Option and Core

- 3Gbps non-blocking packet switching and multicasting
- Three 10/100/1000 Mbps Ethernet ports via SGMII/serial
- Two 10/100 Mbps Ethernet ports via SMII/MII
- Eight E1/T1/J1 direct LIU interfaces
- External DDR2/DDR3 SDRAM for packet memory, control memory, packet look-up memory
- Provides synchronous generic 16-bit CPU interface

Ethernet/VLAN/PBT and OAM

- Supports MEF E-LAN, E-Line, E-Tree and PWE-3
- Complies with IEEE 802.1D, 802.1p, 802.1Q, 802.1ad, 802.1ah and 802.3ah
- Support Link Aggregation conform to IEEE 802.3ad with up to 8 switch ports
- Supports double VLAN tagging/Q-in-Q
- Supports MAC-in-MAC conform to IEEE 802.1ah (PBB) and PBT/PBB-TE
- Supports jumbo frame up to 14000 bytes
- Provides MAC learning and aging, up to 8K MACs
- Supports up to 4k VLAN lookup table
- Provides Ethernet multicast and broadcast with full-speed
- Provides multicast storm control
- Accelerates Rapid Spanning Tree and Multi Spanning Tree protocols
- Supports IGMP snooping (version 1, 2, 3), GVRP snooping and GMRP snooping
- Accelerates Link OAM and CFM OAM processing and loopback (IEEE 802.3ah and 802.1ag)

MPLS/VPLS/MPLS-TP

- Supports MPLS, VPLS and PWE-3
- Up to 8K MPLS labels lookup table
- Up to 8K E-Lines/PWE-3 pseudo wires
- Supports up to 3 push and pops per packet for MPLS label or/and VLAN
- Provides MPLS TTL handling
- Accelerates MPLS OAM, MPLS VCCI, MPLS BFD processing
- Support MPLS-TP protocol

Device and Software

- Implemented in low-cost Altera FPGA device
- Easy in upgrade, integration, feature customizations, enhancements and updated packet protocols
- Easy to design as an ASSP device
- One API software driver for the whole family of devices
- High-level API software driver architecture approach
- Platform independent and Operation System independent

Quality of Service

- Provides a set of packet classification, policing, queuing and scheduling for Quality of Service
- Flows selected from flexible flow selection by port, MPLS, C-VLAN and S-VLAN
- Up to 8 Classes of Service selected from MPLS Exp, VLAN priority and IP DS field
- Policing per flow basis in compliance with MEF 10 technical specification based on 512 profiles
- Supports MEF color aware and color blind policing
- Supports Weighted Random Early Drop (WRED) with 4 drop precedence levels
- Advanced hierarchy shaping per output queue and per output port in a granularity of 1Mbps
- Advanced scheduling with strict priority and weighted round robin
- Provides various per-flow statistic counters

Protection and Redundancy

- Supports sub 50ms protection switching time
- Supports Ethernet protection modes: Ethernet link aggregation, spanning tree, rapid spanning tree (STP,RSTP,MSTP), Ethernet1+1, 1:1 (G.8031), ring protection (G.8032)
- Supports MPLS 1+1, 1:1 protection

Timing and Pseudowire

- Supports synchronous Ethernet
- Supports Ethernet PW over MPLS
- Supports E1/T1/J1 SAToP over Ethernet, MPLS, IPv4 and IPv6

E1/T1 SAToP

- Supports SAToP according to RFC4553, Y.1413, Y.1453, MFA 8.0, MEF 8 without octet-aligned mode
- Provides jitter buffer for Packet Delay Variation (PDV) tolerance, packet re-ordering and clock recovery from PSN
- Programmable size up to 64ms of jitter buffer to optimize delay of each connection in order to meet standard requirements

Timing and Clock Recovery from PSN

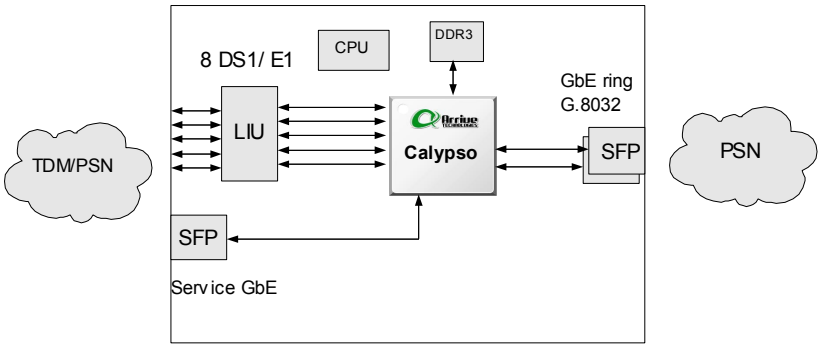
- Supports ACR (Adaptive Clock Recovery) to meet jitter and wander requirements in G.8261, G.823 and G.824
- Built-in DPLL for E1/T1/J1 clock recovery from PSN with locking, hold-over, free-run and power-down modes
- Rich set of timing modes: packet timing, internal timing and loop timing
- Accepts timing packet stream with offsets from 100pps to 8000pps

Carrier Grade Diagnostic

- Supports various loopback modes for interfaces, flows
- Supports internal BERT engines for testing and diagnostic purposes
- Supports error detection on external RAMs

Application Samples

Pizza-box, Carrier Ethernet, Service Side is TDM and Gigabit Ethernet



Pizza-box, Carrier Ethernet, Ethernet Demarcation