



GENERAL DESCRIPTION

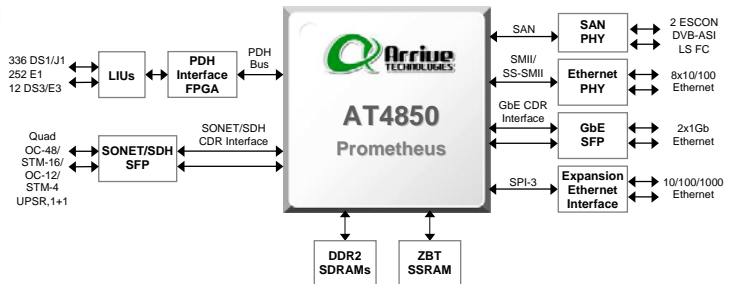
The AT4850 provides a multi-format and multi-rate Ethernet and common legacy data over PDH, PDH mapped to SONET/SDH or direct SONET mapping. On the PDH side, the chip provides a parallel multiplexed PDH bus carrying 12 DS3s or 12 E3s or 336 DS1s or 252 E1s or any mixture of them. A simple FPGA is used to convert parallel DS1/E1/DS3/E3 signals on the PDH bus to the serial signals required for the LIUs for pin count expansion. The 336DS1/252E1s signals can be accessed directly on the PDH bus or be multiplexed to 12 channelized DS3/E3s via 12 embedded M13/E13 engines or mapped to SONET/SDH. The chip supports a quad OC-48/STM-12/OC-12/STM-4 SONET/SDH interface with 1+1 protection, UPSR and mapping of DS1/E1/DS3/E3 to SONET/SDH. On the Ethernet side, the chip provides 8 Fast Ethernet via SMII/SS-SMII bus and 2 Gigabit Ethernet ports with on-chip CDRs. It also supports an OIF SPI-3 bus to support external devices such as a Packet Switches, Network Processor to provide extended L2+ or L3 level processing or expansion of the Ethernet ports. The AT4850 supports ATM, GFP-T/F, HDLC, PPP and LAPS encapsulation. A Traffic Aggregation and Management at Layer 2 for VLAN/MPLS with Classifying, Policing, Queuing, Shaping, and Scheduling is provided. It provides direct SONET/SDH mapping, SONET/SDH/PDH virtual concatenation (VCAT) and LCAS with 128 groups in accordance with G.7041, G.8040, G.7042 and G.7043. The AT4850 includes flexible channel assignment for all applicable SDH and SONET mappings. Two serial ports are provided for ESCON, DVB-ASI or low speed Fiber Channel SAN applications.

KEY FEATURES

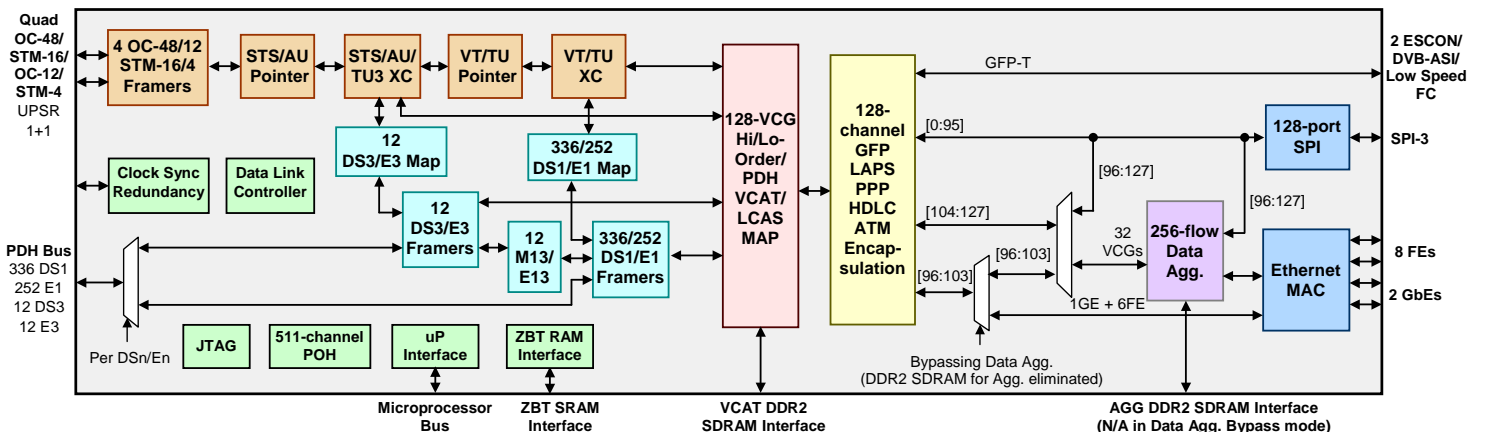
- ❑ Eight 10/100Mbps Ethernet ports via SMII/SS-SMII
- ❑ Two 1Gbps Ethernet ports with on-chip CDR
- ❑ Two ESCON/DVB-ASI/Low Speed FC (200/270/531Mbps) port with serial clock and data interface
- ❑ 128 Logical ports SPI-3 interface for Ethernet expansion
- ❑ Quad multi-rate OC-48/STM-16/OC-12/STM-4 ports with on-chip CDR
- ❑ 12 DS3/E3s, or 336 DS1s, or 252 E1s or any mixture of them on a multiplexed PDH bus
- ❑ Ethernet MAC controller with flow control including jumbo frame
- ❑ Support 802.3ah Ethernet OAM processing and loopback
- ❑ 128 Hi/Lo-Order/PDH VCAT channels with external memory supported delay compensation and on-the-fly programmable differential delays for each VCAT channel
- ❑ Each VCAT channel supports differential delay with up to 384ms for DS1s, up to 256ms for E1/E3s and up to 217ms for DS3s, up to 256ms of STS/VC/VT/TU
- ❑ LCAS with hitless add/remove and fault isolation
- ❑ GFP-F/T, PPP/HDLC, LAPS and ATM encapsulation
- ❑ Traffic Aggregation and Management at Layer 2 for VLAN/MPLS with Classifying, Policing, Queuing, Shaping, and Scheduling
- ❑ Eliminates an external packet SDRAM for transportation of Ethernet ports over PDH without statistical multiplexing
- ❑ 12 DS3 C-bit Parity and DS3 M13 multiplexing
- ❑ 12 E3 G.832 and E3 G.751 E13 multiplexing
- ❑ 336 DS1 SF/ESF Framers supporting J1 SF/ESF
- ❑ 252 E1 basic frame or CRC-4 multi-frame framers
- ❑ Mapping of 336DS1/252E1 and 12DS2/E3 to SONET/SDH
- ❑ 2x32Mx16 DDR2 SDRAM for VCAT delay compensation (can be eliminated if VCAT is not utilized)
- ❑ 3x32Mx16 DDR2 SDRAM for Data Aggregation buffer (can be eliminated if Data Aggregation is not utilized)
- ❑ 1x512Kx36 ZBT SSRAM for hardware status
- ❑ Provided in an HFC-BGA1296 package
- ❑ Typical power consumption is 7 watts

APPLICATIONS

- ❑ Carrier Ethernet wireless and business aggregation and backhaul systems
- ❑ Customer Premises Data Service aggregation and multiplexers
- ❑ Routers, Switches, Edge Systems, MSPPs and Broadband DLCs
- ❑ NxDS1/E1 carrying packet data from mobile backhaul base stations to transport network
- ❑ NxDS1/E1 over DS3/E3 M13/E13 carrying packet data from mobile backhaul base stations to transport network
- ❑ NxDS3/E3 carrying packet data from Business or Enterprise to transport network



AT4850 BLOCK DIAGRAM





FEATURES SUMMARY

Ethernet MAC

- ❑ Complies with MAC for Gigabit and Fast Ethernet framing, flow control handling and auto-negotiation
- ❑ Support Ethernet OAM processing and loopback in compliant with IEEE 802.3ah
- ❑ IEEE 802.3 flow control protocol over SONET transparently
- ❑ Rate limiting based Rx Ethernet FIFO
- ❑ Jumbo frame support
- ❑ MAC Counters for Ethernet Statistics
- ❑ Optional FCS Insertion at Transmit Ethernet MAC
- ❑ Supports Ethernet OAM extraction and insertion
- ❑ Support EoS/EoPDH/EoPoS with or without Data Aggregation

SPI-3

- ❑ 8-bit/16-bit/32-bit OIF SPI-3 Interface up to 128 physical ports
- ❑ Programmable data segmentation of 64 or 128 bytes providing flexible interface to encapsulation supporting varied data packet protocols
- ❑ SPI-3 to/from Data Aggregation have a LUT which can configure any SPI port to any Aggregation VCG

L2 Aggregation & Management

- ❑ Supports Layer 2 Aggregation with VLAN, VLAN Stacking (QinQ)
- ❑ Supports MPLS pseudowire emulation (PWE)
- ❑ Supports GFP Multiplexing
- ❑ Supports all functions of Aggregation including Classifying, Policing, Queuing, Shaping and Scheduling.
- ❑ Classifying function based on port ID, VLAN ID and priority bits or MPLS via a lookup CAM
- ❑ Policing function based on the MEF10 technical specification from the Metro Ethernet Forum
- ❑ Supports 256 service flows/queues
- ❑ Deficit Weighted Round Robin (DWRR) or Strict Priority Scheduler provided for scheduling
- ❑ Ethernet MAC Class-of-Service (CoS of IEEE 802.1p) and MPLS EXP bits of VC label mapping
- ❑ MPLS label stack with Virtual Connection Label (VCL) and Tunnel Label (TL) in accordance with the IETF

Data Encapsulation

- ❑ ATM, GFP, PPP/HDLC, LAPS simultaneously, full-duplex 128 channels
- ❑ ATM, GFP, PPP/HDLC, LAPS mapping to PDH in compliance with G.8040, X.85/86 and G.804
- ❑ Supports Fiber Channel (FC), ESCON, DVB-ASI over SONET/SDH via GFP-T
- ❑ Complies with ITU-T I432.2 (ATM), ITU-T G.7041 (GFP), RFC-1619/1662/2615 (PPP), ITU-T X.85/86 (LAPS), HDLC mapping standards
- ❑ Cell HEC and packet FCS checker/generator and 1-bit HEC error correction
- ❑ Idle/unassigned cell, aborted sequence detection/generation
- ❑ Cell/packet payload scrambling/de-scrambling
- ❑ Bit stuffing and byte stuffing on PPP and HDLC
- ❑ Supports rate adaptation for LAPS/HDLC/PPP
- ❑ Extraction and insertion header field support
- ❑ Supports frame extraction and Insertion
- ❑ Supports 16 or 32 bit HDLC frame check sequence field (FCS) per channel

Datalink Controller

- ❑ 512 standard HDLC channels
- ❑ DCC bytes from SONET/SDH framers
- ❑ Bit-oriented Message and Facility Data Link from PDH framers
- ❑ Data Link in K3 bytes from Path Overhead (POH) processor
- ❑ Flexible datalink buffer setup and management significantly offloading host processor from real time demands from the large channel count

Redundancy Controller

- ❑ 10Mbps redundancy data link
- ❑ Active/standby switchover under software control

VCAT & LCAS

- ❑ 336DS1/252E1/12DS3/12E3 of PDH termination, STS-48 of STS/VC termination, and STS-12 VT/TU termination via 128 channels
- ❑ Supports PDH VCAT and LCAS in compliance with G.7043
- ❑ Supports Standard Contiguous, any Random and Virtual Concatenation
- ❑ Complies with Link Capacity Adjustment Scheme (LCAS) as in ITU-T G.7041 with hitless addition/removal and fault isolation
- ❑ TUG-3 SDH Concatenation with both VC-4-Xv and VC-3-Xv support
- ❑ Contiguous and Random Concatenation with Hi-order VC-3-Xc (X=1-48), VC-4-Xc (X=1-16), Lo-order VC-2-Xc (X=1-7), VC-12-Xc (X=1-21) and VC-11-Xc (X=1-28)
- ❑ Virtual Concatenation (VCAT) with Hi-order VC-3-Xv (X=1-48), VC-4-Xv (X=1-16), Lo-order VC-2-Xv (X=1-21), VC-12-Xv (X=1-63) and VC-11-Xv (X=1-64).
- ❑ PDH VCAT levels with Nx1544, Nx2048 (N=1-16), Nx34368, Nx44736 (N=1-8)
- ❑ Data mapping over DS1/J1/E1/DS3/E3 in compliance with G.8040, X.85/86 and G.804
- ❑ Supports Data/Ethernet mapping-over-PDH over SONET/SDH
- ❑ Accommodates a PDH VCAT differential delay of 384ms for DS1s, 256ms for E1/E3s, and 217ms for DS3s, 256ms of STS/VC/VT/TU
- ❑ Low optimized packet latency in VCAT De-skew
- ❑ On-the-fly programmable differential delays for each VCAT channel to permit short loop and long international paths
- ❑ SPI-3 interface has a maximum of 128 VCGs for transporting data over PDH/SONET/SDH

SONET/SDH

- ❑ Built-in 4 OC-48/STM-16/OC-12/STM-3 Framers
- ❑ Full SONET/SDH Section/Line Overhead processing
- ❑ Hardware based APS processing for Linear and UPSR
- ❑ Standard Contiguous and any Random Hi-order and Lo-order pointer processing
- ❑ Full STS/VC and VT/TU Path monitoring/termination through a selectable 511-channel pool
- ❑ Full SONET/SDH Line 10-3 to 10-9 hardware BER detection
- ❑ Selectable 511 STS/VC, VT/TU with 10-3 to 10-9 hardware BER detection

STS/AU/VT/TU Cross Connect

- ❑ 348x348 STS-1/VC-3s Cross-connect
- ❑ 48x48 TU3s Cross-connect
- ❑ 2016x2016 VT-1.5/TU-11s Cross-connect

PDH Features

- ❑ Integrates 336 DS1/J1 framers, 252 E1 framers, 12 DS3/E3 framers
- ❑ Implements bit asynchronous mapping of 336 DS1/J1 to VT1.5/TU11 or 252 E1 to VT2/TU12 or any mixed
- ❑ Supports 12 M13/E13 multiplexers with 12 DS3/E3 framers
- ❑ Supports mapping of VT1.5/VT2/TU11/TU12 and DS3/E3 to SONET/SDH SPE
- ❑ DS1/E1 to DS3/E3 Mux, Asynchronous DS1/E1 to VT/TU Map, Asynchronous DS3/E3 to STS1/VC3 Map with Jitter Attenuation
- ❑ Supports PDH VCAT and LCAS in compliance with G.7043
- ❑ PDH multiplexed bus requires external FPGA for mux/demux and external LIUs with jitter attenuation

System Clock Synthesizer

- ❑ Accepts the multiple of 8KHz input reference clock and monitor clock
- ❑ Accepts an 8KHz or 1.544MHz/2.048MHz input reference clock and an 8KHz or 1.544MHz/2.048MHz input monitored clock
- ❑ Selectable clock reference and clock monitoring from SONET/SDH Line or Hi-order or Lo-order path
- ❑ Supports Free-run, Locked, and Holdover modes of operation
- ❑ Supports working/protection clock synchronization with multi-frame phase accuracy of 6.43ns