

## INTRODUCTION

The AT4848 is a highly integrated OC-48/STM-16 or OC-12/STM-4 Multiservice Add/Drop Multiplexer (ADM) on a chip. The device can be used in a variety of next generation data over SONET/SDH systems including Multiservice Provisioning Platforms (MSPP), Broadband Access and Enterprise Customer Premise Equipment with an integrated ADM. The AT4848 has integrated cross-connects supporting DS0, VT/TU and STS/VC level switching. The device includes MACs and framers for a range of drop side interfaces including Fast Ethernet, Gigabit Ethernet, storage and video protocols, SONET/SDH and high density DS1/E1s and DS3/E3s. The AT4848 supports Frame and Transparent GFP mapping, SONET/SDH HI/LO and PDH virtual concatenation (VCAT) and LCAS with 128 groups. The AT4848 provides VLAN/MPLS applications with on-chip L2 Aggregation & Management. An OIF SPI interface is available for expansion through an external network processor, additional Ethernet or RPR MAC. An OIF SPI interface is available for expansion through an external network processor, additional Ethernet or RPR MAC.

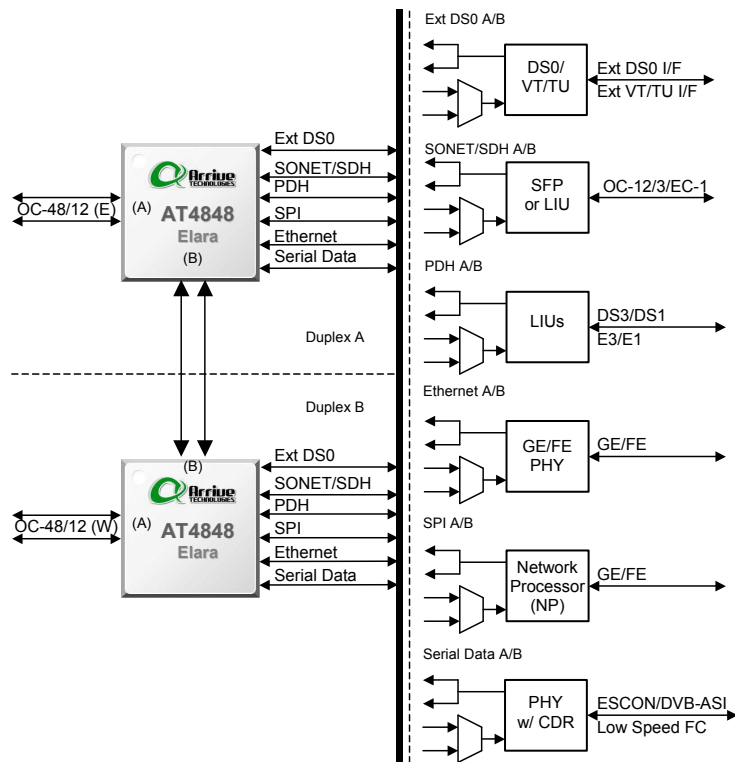
## APPLICATIONS

- ❑ Next Generation MSPP, MSTP or ADM systems
- ❑ Next Generation ultra low cost micro and pizza box MSPPs/ADM
- ❑ Next Generation DSLAM and Triple Play systems with integrated ADM
- ❑ OLT for FSAN, FTTP, FTTN, GPON or EPON systems with integrated ADM/MSPP
- ❑ SONET/SDH Enterprise Customer Premises Equipment with integrated ADM/MSPP
- ❑ Line-cards for SONET/SDH Switches and Cross-connects
- ❑ Multi-rate/multi-format Mapping of Ethernet over PDH or PDH/SONET/SDH
- ❑ Ideal for cost sensitive wireless backhaul and Ethernet/PDH private line backhaul systems

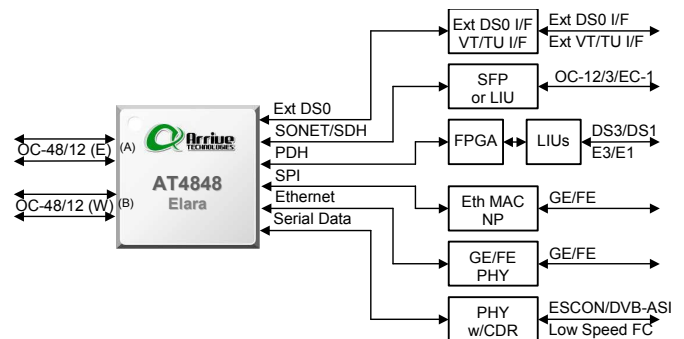
## KEY FEATURES

- ❑ 2.5/.622Gbps SONET/SDH Data & PDH Multi-Service ADM on a chip
- ❑ 4xOC-48/STM-16 or OC-12/STM-4 SONET/SDH network interfaces
- ❑ Supports Hardware based APS for Linear and UPSR/SNCP
- ❑ Incorporates a 20 Gbps STS/VC, 2.5 Gbps TU3, 5 Gbps VT1.5/VT2/VT3/VT6/TU11/TU12/TU2, and 8K DS0 Cross-connects
- ❑ Integrated Fast Ethernet and Gigabit Ethernet, FC/FICON/ESCON and DVB-ASI ports
- ❑ Supports 128 SONET/SDH HI/LO and PDH VCAT Groups with LCAS
- ❑ Transparent and Frame GFP mapping
- ❑ OIF SPI-3 port with up to 128 logical channels
- ❑ Integrated 12xDS3/E3 and 336/252xDS1/E1 framers
- ❑ Integrated Drop side framers for 4xOC-12/STM-4s, 4xOC-3/STM-1s or 12xOC-3/STM-1s/EC-1s
- ❑ Traffic Aggregation and Management at Layer 2 for VLAN/MPLS with Classifying, Policing, Queuing, Shaping and Scheduling
- ❑ E-LAN/VPLS is supported via an external FPGA or ASIC connected at SPI-3 port
- ❑ Integrated system clock synchronization
- ❑ ZBT RAM Interface for HDLC controller, DS0 signaling processor, and BER storage
- ❑ DDR2 SDRAM Interface for VCAT de-skewing and packet buffering
- ❑ Provided in an HFC-BGA1296 package
- ❑ Typical power consumption is 8.5 watts

## Duplex Micro-MSPP



## Simplex Micro-MSPP



**ADM FEATURES**

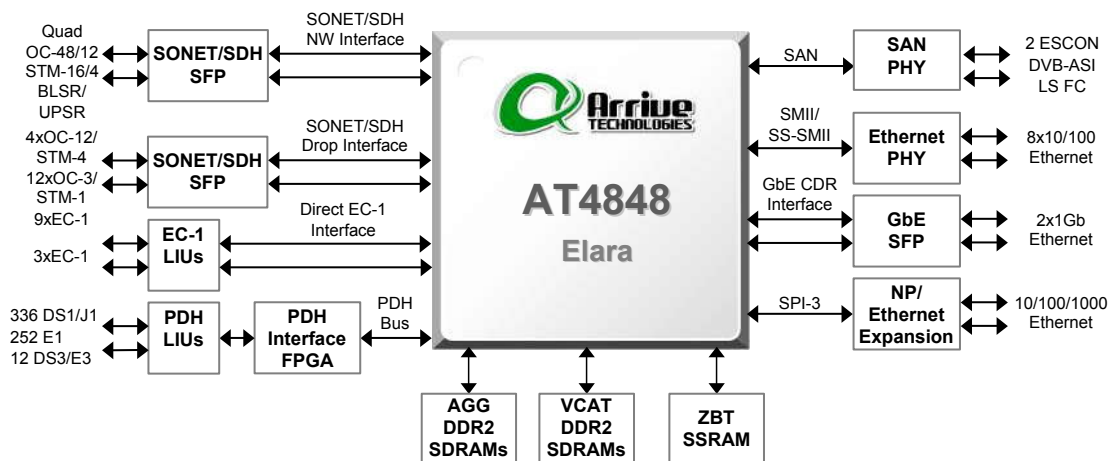
- ❑ 4 individual OC-48/STM-16/OC-12/STM-4 Network Interface ports with on-chip CDR
- ❑ 4 individual OC-12/STM-4/OC-3/STM-1 ports with on-chip CDR
- ❑ 3 serial EC-1/STM-1 ports with on-chip B3ZS Encoder/Decoder
- ❑ SONET/SDH Section/Line Overhead Processor
- ❑ Hardware based Line and Path APS for SONET/SDH
- ❑ SONET/SDH Line BER monitoring ( $10^{-3}$  to  $10^{-9}$ )
- ❑ SONET/SDH 128-channel TOH Transparency pool
- ❑ STS/VC Pointer Processor with standard and random concatenations
- ❑ TU3 Pointer Processor
- ❑ VT/TU Pointer Processor with standard and random concatenations
- ❑ HI/LO 511-channel POH Processor pool
- ❑ 511-channel Tandem Connection Processor pool
- ❑ SONET/SDH HI/LO 511-channel BER monitor pool ( $10^{-3}$  to  $10^{-9}$ )
- ❑ Flexible TOH and POH Add/Drop port
- ❑ 20Gbps 384x384 STS/VC High Order Cross-connect
- ❑ 5Gbps 2688x2688 VT/TU Low Order Cross-connect
- ❑ 48x48 TU3 Cross-connect
- ❑ 8K DS0s and associated Signaling Cross-connect
- ❑ 512-channel HDLC pool of DCC, PDH Facility Data Link, CCS channel, Local Data Link and Redundancy Data Link
- ❑ Clock synthesizer and system active/standby synchronizer

**DATA FEATURES**

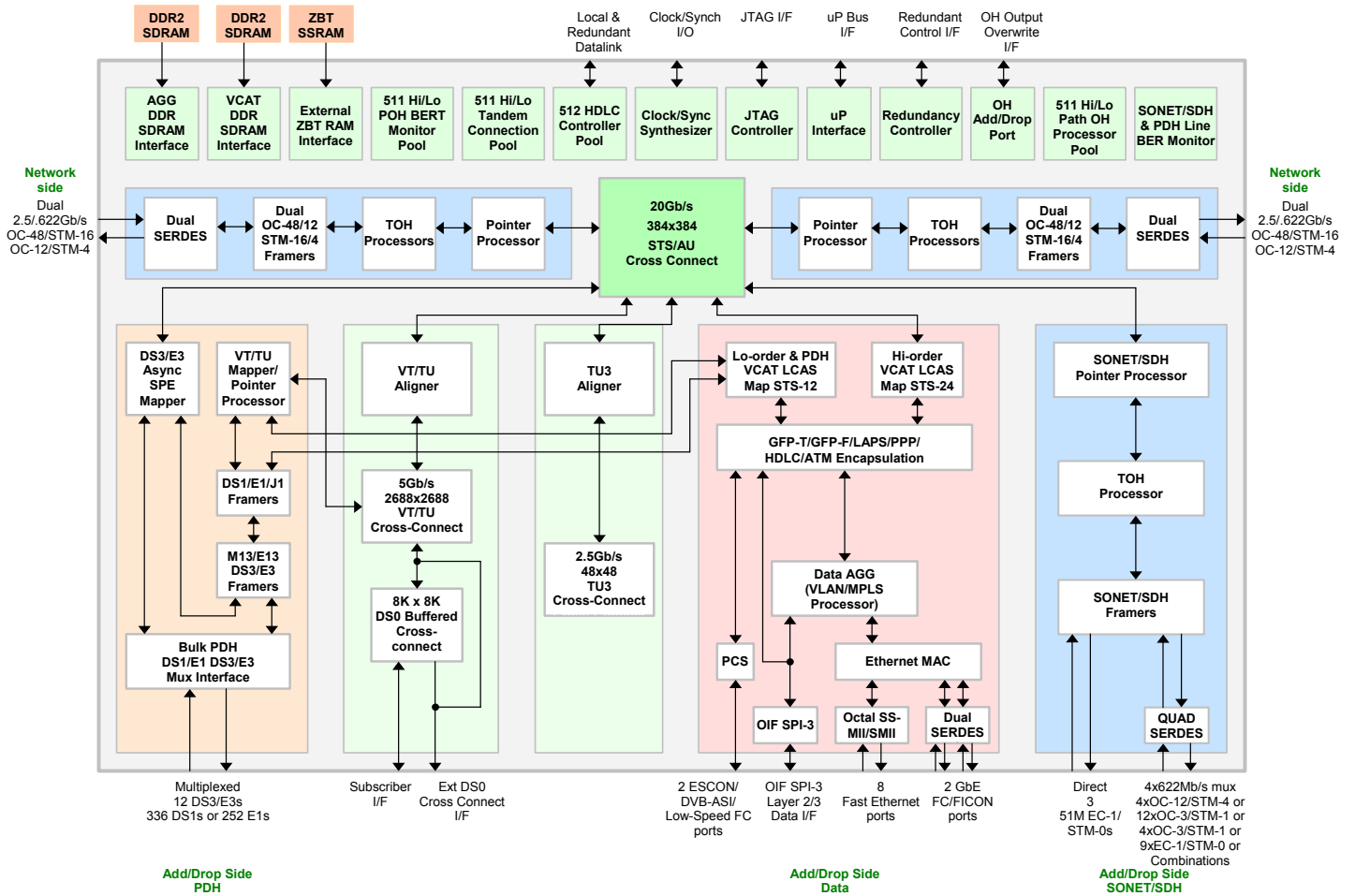
- ❑ 2 GbE/FICON/FC ports with on-chip dual-rate (1.25/1.0625Gbps) CDR
- ❑ 2 ESCON/DVB-ASI/Low Speed FC (200/270/531Mbps) ports with serial clock and data interface
- ❑ 8 Fast Ethernet ports via SMII or SS-SMII
- ❑ OIF SPI-3 Interface up to 128 physical ports with programmable data segmentation of 64 or 128 bytes
- ❑ Ethernet MAC controller with flow control including jumbo frame
- ❑ 128 Hi/Lo-Order/PDH VCAT channels
- ❑ Supports VCAT differential delay with up to 256ms for Hi/Lo-Order, up to 384ms for DS1s, up to 256ms for E1/E3s and up to 217ms for DS3s
- ❑ Supports LCAS with hitless add/remove and fault isolation
- ❑ GFP-T/F, PPP/HDLC, LAPS and ATM encapsulation
- ❑ TUG-3 (SDH concatenation with both VC-4-Xv and VC-3-Xv) supported
- ❑ Data mapping-over- DS1/E1/DS3/E3 over SONET/SDH supported for up to STS-12 bandwidth
- ❑ Traffic Aggregation and Management at Layer 2 for VLAN/MPLS with Classifying, Policing, Queuing, Shaping, and Scheduling
- ❑ Large DDR2 SDRAM for Packet Buffers

**PDH FEATURES**

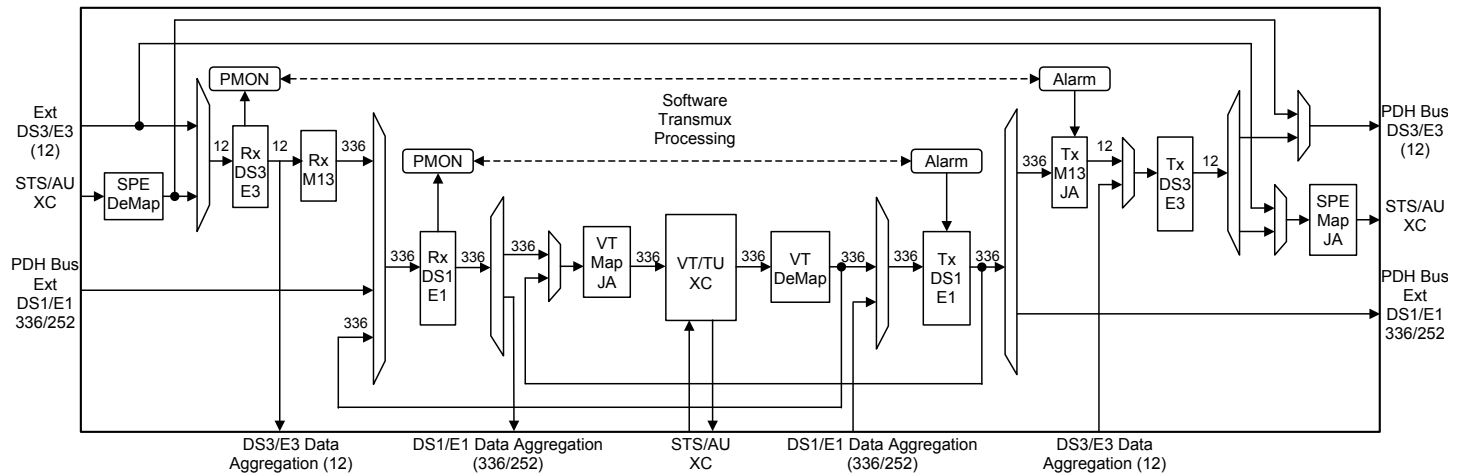
- ❑ Multiplexed 12 DS3/E3s, or 336 DS1s, or 252 E1s or any mixed PDH bus
- ❑ 12 DS3 C-bit Parity and DS3 M13 multiplexing
- ❑ 12 E3 G.832 and E3 G.751 E13 multiplexing
- ❑ Asynchronous mapping 12 DS3/E3 to 12 STS-1/VC-3 SPE
- ❑ 336 DS1 SF/ESF/SLC-96/ DDS Framers supporting J1 SF/ESF
- ❑ 252 E1 basic frame or CRC-4 multi-frame framers
- ❑ Synchronous/Asynchronous mapping 336/252 DS1/E1 to VT1.5/VT2 (or TU-11/TU-12)
- ❑ 8064-DS0 Signaling Processor for Signaling Scan and Dial Pulse Collection
- ❑ DS3/E3, DS1/E1 LCV-based BER monitoring ( $10^{-3}$  to  $10^{-9}$ )
- ❑ PDH through path Jitter Attenuation
- ❑ PDH transmultiplexing to/from SONET/SDH
- ❑ PDH VCAT and LCAS in compliance with G.7043



**BLOCK DIAGRAM**



**PDH Processing Structure**





## FEATURES SUMMARY

### SONET/SDH Interface

- ❑ Built-in 4 OC-48/STM-16 Framers, 4 OC-12/STM-4 Framers, 12 OC-3/STM-1 Framers, and 12 EC-1 Framers. Any port can be used for line or add/drop
- ❑ Full SONET/SDH Section/Line Overhead processing
- ❑ Hardware based APS-L processing for Linear
- ❑ Hardware based UPSR/SNCP processing
- ❑ Standard Contiguous and any Random Hi-order and Lo-order pointer processing and alignment
- ❑ Full STS/VC and VT/TU Path monitoring/termination through a selectable 511-channel pool
- ❑ Selectable 511 SONET/SDH Hi-order and Lo-order Tandem Connection Monitoring (TCM) for both Sink and Source
- ❑ Full SONET/SDH Line  $10^{-3}$  to  $10^{-9}$  hardware BER detection
- ❑ Selectable 511 STS/VC, VT/TU with  $10^{-3}$  to  $10^{-9}$  hardware BER detection
- ❑ Full TOH and flexible 64 POH channels add/drop port
- ❑ Selectable 128 STS-1 Transport Overhead (TOH) Transparency
- ❑ Hitless backplane switching

### PDH Interface

- ❑ Integrates 336 DS1/J1 framers, 252 E1 framers, 12 DS3/E3 framers
- ❑ Implements bit asynchronous or byte synchronous mapping of 336 DS1/J1 to VT1.5/TU11 or 252 E1 to VT2/TU12 or any mixed
- ❑ Supports 12 M13/E13 multiplexers with 12 DS3/E3 framers
- ❑ Supports mapping of VT1.5/VT2/TU11/TU12 and DS3/E3 to SONET/SDH SPE
- ❑ DS1/E1 to DS3/E3 Mux, Asynchronous DS1/E1 to VT/TU Map, Asynchronous DS3/E3 to STS1/VC3 Map with Jitter Attenuation
- ❑ PDH Transmultiplexing to/from SONET/SDH
- ❑ Jitter Attenuation for through path PDH signals
- ❑ Supports PDH VCAT and LCAS in compliance with G.7043
- ❑ PDH multiplexed bus requires external FPGA for mux/demux and external LIUs with jitter attenuation

### Data Interfaces and Processing

#### VCAT & LCAS

- ❑ STS-48 of STS/VC termination and STS-12 of mixed VT/TU and PDH termination via 128 channels
- ❑ Implements Standard Contiguous, any Random and Virtual Concatenation.
- ❑ Supports PDH VCAT and LCAS in compliance with G.7043
- ❑ Complies with Link Capacity Adjustment Scheme (LCAS) as in ITU-T G.7041 with hitless addition/removal and fault isolation
- ❑ TUG-3 SDH Concatenation with both VC-4-Xv and VC-3-Xv support
- ❑ Contiguous and Random Concatenation with Hi-order VC-3-Xc (X=1-48), VC-4-Xc (X=1-16), Lo-order VC-2-Xc (X=1-7), VC-12-Xc (X=1-21) and VC-11-Xc (X=1-28)
- ❑ Virtual Concatenation (VCAT) with Hi-order VC-3-Xv (X=1-48), VC-4-Xv (X=1-16), Lo-order VC-2-Xv (X=1-21), VC-12-Xv (X=1-63) and VC-11-Xv (X=1-64).

#### VCAT & LCAS (Cont.)

- ❑ VCAT levels with Nx1544, Nx2048 (N=1-16), Nx34368 and Nx44736 (N=1-8)
- ❑ Data mapping over DS1/J1/E1/DS3/E3 in compliance with G.8040, X.85/86 and G.804
- ❑ Data mapping-over-PDH over SONET/SDH
- ❑ Accommodates a SONET/SDH VCAT differential delay of 256ms
- ❑ Accommodates a PDH VCAT differential delay of 384ms for DS1s, 256ms for E1/E3s, and 217ms for DS3s
- ❑ Supports VCAT differential delay via a DDR2 SDRAM up to 256Mbytes
- ❑ Low latency in VCAT De-skew
- ❑ On-the-fly programmable differential delays for each VCAT channel to permit short loop and long international paths
- ❑ Aggregation ports and an SPI-3 interface utilize a shared resource with a maximum of 128 VCGs for transporting data over SONET/SDH. The maximum number of logical ports used for Aggregation is 32 VCGs

#### Data Encapsulation

- ❑ ATM, GFP, PPP/HDLC, LAPS simultaneously, full-duplex 128 channels
- ❑ Performs GbE over SONET/SDH via GFP-T framing or Gigabit Ethernet MAC
- ❑ GFP/HDLC/PPP/LAPS/ATM mapping to PDH in compliance with G.8040, X.85/86 and G.804
- ❑ Supports Fiber Channel (FC), FICON, ESCON, Ethernet, DVB-ASI via GFP-T
- ❑ Complies with ITU-T I432.2 (ATM), ITU-T G.7041 (GFP), RFC-1619/1662/2615 (PPP), ITU-T X.85/86 (LAPS), HDLC/Cisco HDLC mapping standards
- ❑ Cell/Frame HEC and packet FCS checker/generator and 1-bit HEC error correction
- ❑ Idle/unassigned cell, aborted sequence detection/generation
- ❑ Cell/packet payload scrambling/de-scrambling
- ❑ Supports rate adaptation for LAPS/HDLC/PPP
- ❑ Bit stuffing and byte stuffing on PPP and HDLC
- ❑ Extraction and insertion header field
- ❑ Supports cell/frame extraction and insertion
- ❑ Supports 16 or 32 bit HDLC frame check sequence field (FCS) per channel
- ❑ Supports ATM idle cell discard or pass-through
- ❑ Statistic counters per data channel, including:
  - Good frame/cell counter
  - FCS/CRC/HEC error counter
  - Single bit HEC error correction counter
  - Abort sequence detection counter
  - Frame length violation counter
  - Frame drop/discard event counter
  - Idle frame/cell counter
  - Transmit underrun counter
  - Out of frame/cell delineation event
  - Loss of cell delineation event

## L2 Aggregation & Management

- ❑ Supports Layer 2 Aggregation with VLAN, VLAN Stacking (QinQ)
- ❑ Supports MPLS pseudowire emulation (PWE)
- ❑ Supports GFP Multiplexing
- ❑ Supports all functions of Aggregation including Classifying, Policing, Queuing, Shaping and Scheduling.
- ❑ Classifying function based on port ID, VLAN ID and priority bits or MPLS via a lookup CAM
- ❑ Policing function based on the MEF5 technical specification from the Metro Ethernet Forum
- ❑ Supports 256 service flows/queues
- ❑ Deficit Weighted Round Robin (DWRR) or Strict Priority Scheduler provided for scheduling
- ❑ Ethernet MAC Class-of-Service (CoS of IEEE 802.1p) and MPLS EXP bits of VC label mapping
- ❑ MPLS label stack with Virtual Connection Label (VCL) and Tunnel Label (TL) in accordance with the IETF drafts

## Ethernet MAC

- ❑ Complies with MAC for Gigabit and Fast Ethernet framing, flow control handling and auto-negotiation
- ❑ IEEE 802.3 flow control protocol over SONET transparently
- ❑ Rate limiting based Rx Ethernet FIFO
- ❑ Jumbo frame support
- ❑ MAC Counters for Ethernet Statistics
- ❑ Optional FCS Insertion at Transmit Ethernet MAC
- ❑ Supports Ethernet OAM extraction and insertion
- ❑ Support 802.3ah Ethernet OAM processing
- ❑ Support EoS with or without Data Aggregation

## Data Link Controller

- ❑ 512 standard HDLC channels
- ❑ DCC bytes from SONET/SDH framers
- ❑ Bit-oriented Message and Facility Data Link from PDH framers
- ❑ Data Link in N1/K3 bytes from Path Overhead (POH) processor
- ❑ Common Channel Signaling (CCS) from DS1/E1 framer
- ❑ ISDN D-channel data link support
- ❑ Local internal system data link support
- ❑ Redundancy data link support

## Redundancy Controller

- ❑ 10Mbps redundancy data link
- ❑ Active/standby switchover under software control

## STS/AU Cross Connect

- ❑ Full, non-blocking 20Gbps TSI Cross-connect for 8 STS-48s or 384x384 at STS-1/VC-3 level
- ❑ STS/VC path select for UPSR/SNCP
- ❑ Multicast and broadcast on per STS-1/VC-3 basis
- ❑ Data loop-back at the add/drop side for ring pass-through data

## TU3 Cross Connect

- ❑ Full, non-blocking 2.5Gbps Cross-connect for 48x48 TU3s
- ❑ Supports TU3 Path Select for UPSR/SNCP Application
- ❑ Supports Multicast and Broadcast on per TU3 basis

## VT/TU Cross Connect

- ❑ 5Gbps Cross-connect for 2688x2688 VT-1.5/TU-11s
- ❑ Supports cross-connect for all types of VT/TU except TU3
- ❑ Supports VT/TU Path Select for UPSR/SNCP Application
- ❑ Supports Multicast and Broadcast on per VT-1.5/TU-11 basis

## DS0 Cross Connect

- ❑ Random, full, non-blocking TSI Cross-connect for 8064 DS0s (STS-12) and ABCD channel associated signaling (CAS)
- ❑ Multicast and broadcast support on per DS0 basis
- ❑ Supports 2-bit D-channel Cross-connect for ISDN
- ❑ Signaling processor for ABCD signaling scan, dial pulse collector, signaling de-bounce, signaling freeze and signaling conversion for 8064 DS0s

## System Clock Synthesizer

- ❑ Suitable for Stratum Level-3 SONET/SDH Equipment Timing Source (SETS) applications
- ❑ Accepts the multiple of 8KHz input reference clock and monitor clock
- ❑ Accepts an 8KHz or 1.544MHz/2.048MHz input reference clock and an 8KHz or 1.544MHz/2.048MHz input monitored clock
- ❑ Selectable clock reference and clock monitoring from SONET/SDH Line or Hi-order or Lo-order path
- ❑ Supports Free-run, Locked, and Holdover modes of operation
- ❑ Supports working/protection clock synchronization with multi-frame phase accuracy of 6.43ns