



AT4825

OC-48 Multi-Service ADM Lite



Rev. 1.3 – May 2008

Preliminary Short Data Sheet

INTRODUCTION

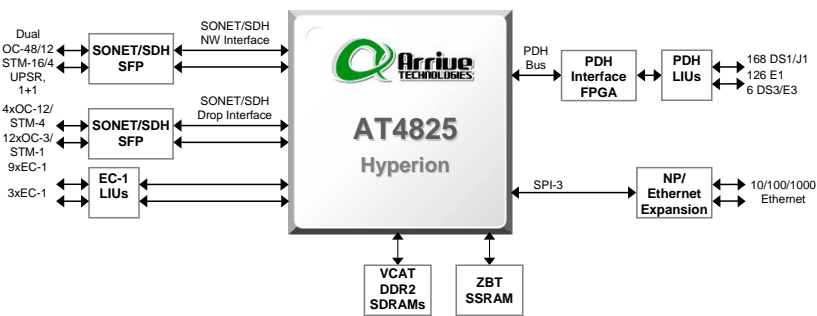
The AT4825 is a highly integrated OC-48/STM-16 or OC-12/STM-4 Multiservice Add/Drop Multiplexer on a chip. The AT4825 has integrated cross-connects supporting VT/TU/TU3 and STS/VC level switching. The AT4825 provides a multi-format and multi-rate Ethernet and common legacy data over PDH, PDH mapped to SONET/SDH or direct SONET mapping via a SPI-3 interface. On the PDH side, the chip provides a parallel multiplexed PDH bus carrying 6 DS3s or 6 E3s or 168 DS1s or 126 E1s or any mixture of them. The 168/126 DS1/E1s signals can be accessed directly via the PDH bus or be multiplexed to 6 channelized DS3/E3s via 6 embedded M13/E13 engines or mapped to SONET/SDH. The chip supports dual OC-48/12 or STM-16/4 SONET/SDH interface with linear 1+1 or UPSR/SNCP hardware managed protection. It supports an OIF SPI-3 bus to support external devices such as a Network Processor to provide extended L2+ or L3 level processing or direct Ethernet ports. The AT4825 supports ATM, GFP-T/F, HDLC, PPP and LAPS encapsulation. It provides direct SONET/SDH mapping, SONET/SDH/PDH virtual concatenation (VCAT) and LCAS with 128 groups in accordance with G.7041, G.8040, G.7042 and G.7043.

APPLICATIONS

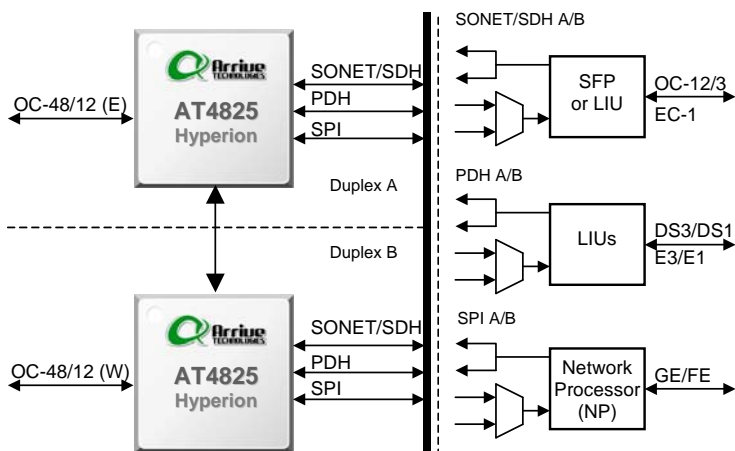
- Next Generation MSPP, MSTP or ADM systems
- Next Generation ultra low cost micro and pizza box MSPPs/ADMs
- SONET/SDH Enterprise Customer Premises Equipment with integrated ADM/MSPP
- Line-cards for SONET/SDH Switches and Cross-connects
- Multi-rate/multi-format Mapping of Ethernet over PDH or PDH/SONET/SDH
- Ideal for cost sensitive wireless backhaul and Ethernet/PDH private line backhaul systems

KEY FEATURES

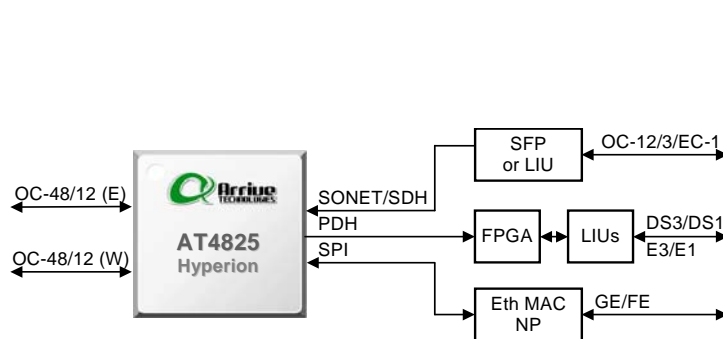
- 2.5 Gbps SONET/SDH Data & PDH Multi-Service ADM on a chip
- 2xOC-48/STM-16 or OC-12/STM-4 SONET/SDH network interfaces
- 4xOC-12/STM-1 or OC-3/STM-1 SONET/SDH drop interfaces
- 622Mbps/155Mbps SONET/SDH drop interface for 9xEC-1 or 12 OC-3/STM-1
- 3xEC-1 serial drop interfaces
- Supports Hardware based APS for Linear and Ring networks including UPSR/SNCP
- Includes STS/VC, TU3, VT1.5/VT2/VT3/VT6/ TU11/TU12/TU2 Cross-connects
- Supports 128 SONET/SDH HI/LO and PDH VCAT Groups with LCAS
- OIF SPI-3 port with up to 128 logical channels
- Integrated 6xDS3/E3 and 168/126xDS1/E1 framers
- Integrated Network side framers for 2xOC-48/ STM-16 or OC-12/STM-1s
- Integrated Drop side framers for 4xOC-12/STM-4, 4xOC-3/STM-1s or 12 OC-3/STM-1/EC-1s
- Integrated system synchronization
- 2x32Mx16 DDR2 SDRAM for VCAT delay compensation (can be eliminated if VCAT is not utilized)
- 1x512Kx36 ZBT SSRAM for hardware status
- Provided in an HFC-BGA1296 package
- Typical power consumption is 6 watts



Duplex MSPP



Simplex MSPP





SYSTEM FEATURES

- ❑ 2 OC-48/STM-16/OC-12/STM-4 Network Interface ports with on-chip CDR
- ❑ 4 individual OC-12/STM-4/OC-3/STM-1 ports with on-chip CDRs
- ❑ 4x622Mbps/155Mbps port with on-chip CDR for 12xOC-3 and 9xEC-1
- ❑ 3 serial EC-1 ports with on-chip B3ZS Encoder/Decoder
- ❑ SONET/SDH Section/Line Overhead Processor
- ❑ Hardware based Line and Path APS for SONET/SDH
- ❑ SONET/SDH Line BER monitoring (10-3 to 10-9)
- ❑ Full SONET/SDH TOH Transparency
- ❑ STS/VC Pointer Processor with standard and random concatenations
- ❑ TU3 Pointer Processor
- ❑ VT/TU Pointer Processor with standard and random concatenations
- ❑ Hi-order/Lo-order 511-channel POH processor pool
- ❑ 511-channel Tandem Connection Monitor pool
- ❑ SONET/SDH Hi-order/Lo-order 511-channel BER monitor pool (10-3 to 10-9)
- ❑ Flexible TOH and POH Add/Drop port
- ❑ 288x288 STS/VC High Order Cross-connect
- ❑ 1848x1848 VT/TU Low Order Cross-connect
- ❑ 48x48 TU3 Cross-connect
- ❑ 512-channel HDLC pool of DCC, PDH Facility Data Link, CCS channel, Local Data Link, and Redundancy Data Link
- ❑ Clock synthesizer and system active/standby synchronizer

BLOCK DIAGRAM

DATA FEATURES

- ❑ OIF SPI-3 Interface up to 128 physical ports with programmable data segmentation of 64 or 128 bytes
- ❑ 128 Hi/Lo-Order/PDH VCAT channels, with external memory supported delay compensation and on-the-fly programmable differential delays for each VCAT channel
- ❑ Each VCAT channel supports differential delay with up to 256ms for SONET/SDH HI/LO, up to 384ms for DS1s, up to 256ms for E1/E3s, and up to 217ms for DS3s
- ❑ LCAS with hitless add/remove and fault isolation
- ❑ GFP, PPP/HDLC, LAPS and ATM encapsulation
- ❑ TUG-3 (SDH concatenation with both VC-4-Xv and VC-3-Xv) supported

PDH FEATURES

- ❑ Multiplexed 6 DS3/E3s, or 168 DS1s, or 126 E1s or any mixed PDH bus
- ❑ 6 DS3 C-bit Parity and DS3 M13 multiplexing
- ❑ 6 E3 G.832 and E3 G.751 E13 multiplexing
- ❑ Asynchronous mapping 6 DS3/E3 to 6 STS-1/VC-3 SPE
- ❑ 168 DS1 SF/ESF/SLC-96/DDS Framers supporting J1 and SF/ESF
- ❑ 126 E1 basic frame or CRC-4 multi-frame framers
- ❑ Synchronous/Asynchronous mapping 168/126 DS1/E1 to VT1.5/VT2 (or TU-11/TU-12)
- ❑ DS3/E3, DS1/E1 LCV-based BER monitoring (10-3 to 10-9)
- ❑ PDH through path Jitter Attenuation
- ❑ PDH transmultiplexing to/from SONET/SDH
- ❑ PDH VCAT and LCAS in compliance with G.7043



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