



INTRODUCTION

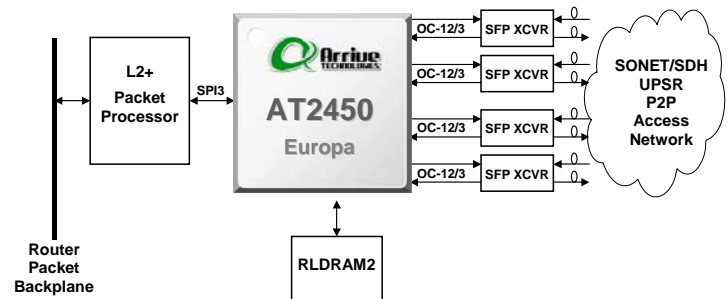
Europa is a high-density deep channelization Multi-protocol processor supporting 2048 channels from STS-12c to DS0 with an aggregate capacity of 1.244Gbps. It allows Ethernet and most data services to be terminated and mapped to/from SONET/SDH and/or PDH channels. EUROPA provides four individually programmable OC-3/STM-1 or OC-12/STM-4 eight bit parallel or serial interfaces with SerDes and CDR. It provides a complete ADM or Terminal for PDH or Data services. It supports deep channelization including any SONET/SDH VCAT payload, 24 DS3/E3s with multi-vendor CSU/DSU subrate and M13/E13 or VT/TU mapped 672/504 DS1, E1, J1s and nxDS0 via an OIF SPI-3 interface. Channelization includes standard-based contiguous, any random and Virtual Concatenation or PDH VCAT and LCAS in compliance with G.7043. These channels may include ITU-T I.432.2 (ATM), ITU-T G.7041 (GFP), RFC-1619/1662/2615 (PPP), ITU-T X.85/86 (LAPS), HDLC or BCP mapped flexibly to SONET or PDH. Encapsulation also includes support for Cisco HDLC, Frame Relay, and Ethernet mapping to either SONET/SDH or PDH. Additional processing for ML FR, ML PPP, IMA, and L2+ can be provided by an external Access/Network Processor via the SPI-3 port.

Data is encapsulated then mapped into the SONET/SDH VCAT VCGs, including the 16k-DS0 or 672/504 DS1/E1/J1 or 24 DS3/E3 channels, and then mapped to the SONET/SDH network interfaces or to external LIUs via a parallel PDH interface. Europa supports a flexible mapping from SPI-3<-> SONET/SDH, SPI-3<-> PDH interface or PDH interface <-> SONET/SDH. The SONET/SDH interfaces include framers, pointer processors and complete TOH and POH processing. The SONET/SDH interfaces support hardware-based SONET/SDH automatic protection switching (APS) and SDH Multiplex Section Protection (MSP) for UPSR/SNCP rings, Linear and P2P. The STS/AU, TU3 and VT/TU cross-connects are provided for ADM and Terminal applications, flexible channel assignment, channel re-arrangement, protection switching, diagnostics and loopbacks.

APPLICATIONS

- ❑ Any Service Any Port - ASAP linecards
- ❑ Channelized PDH and SONET/SDH linecards
- ❑ Multi-Service Edge Switches and Routers
- ❑ Radio Network Controllers
- ❑ Very high-density Ethernet over PDH/SONET/SDH
- ❑ Wireless Backhaul Aggregation Platforms
- ❑ Multi-Service Provisioning Platforms

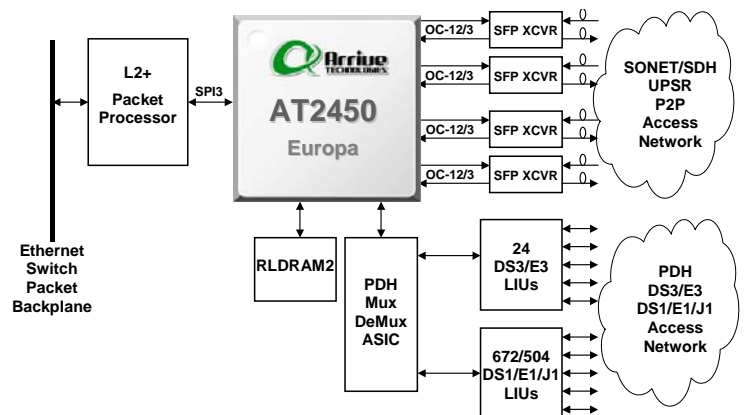
ROUTER / SWITCH / RNC LINECARD



KEY FEATURES

- ❑ 1.244Gbps aggregate capacity deep channelized multi-protocol framer, mapper, processor and L2 termination
- ❑ Provides four OC-12/3 or STM-4/1 independently programmable channelized network interfaces with integrated SerDes w/CDR, full TOH processing and flexible SONET/SDH multiplexing to the nxDS0 level
- ❑ Includes 672/504 DS1/E1 and 24 DS3/E3 multi-framers and STS/VC, TU3 and VT/TU cross-connects supporting full ADM and Terminal capabilities
- ❑ Supports 2048 individual channels, flexibly mapped and encapsulated by GFP/HDLC/Cisco-HDLC/PPP/BCP/LAPS/ATM
- ❑ Supports Frame Relay, Multilink Frame Relay (ML FR) and Multilink Point-to-Point Protocol (ML PPP) in combination with a Network/Access Processor
- ❑ Supports GFP-F encapsulated Ethernet over SONET/SDH, E1, DS1, J1, E3, DS3 VCAT and LCAS in compliance with G.7043 over 672/504 DS1/E1/J1, either VT/TU or M13/E13 mapped plus 24 DS3/E3s
- ❑ Supports hardware-based SONET/SDH automatic protection switching (APS) and SDH Multiplex Section Protection (MSP) for UPSR/SNCP rings, Linear and P2P
- ❑ Subrate and scrambling supported for the following major DSU vendors: Quickeagle (DigitalLink), Kentrox, Adtran, Verilink and Larscom (CSU/DSUs)

ETHERNET-OVER-PDH LINECARD





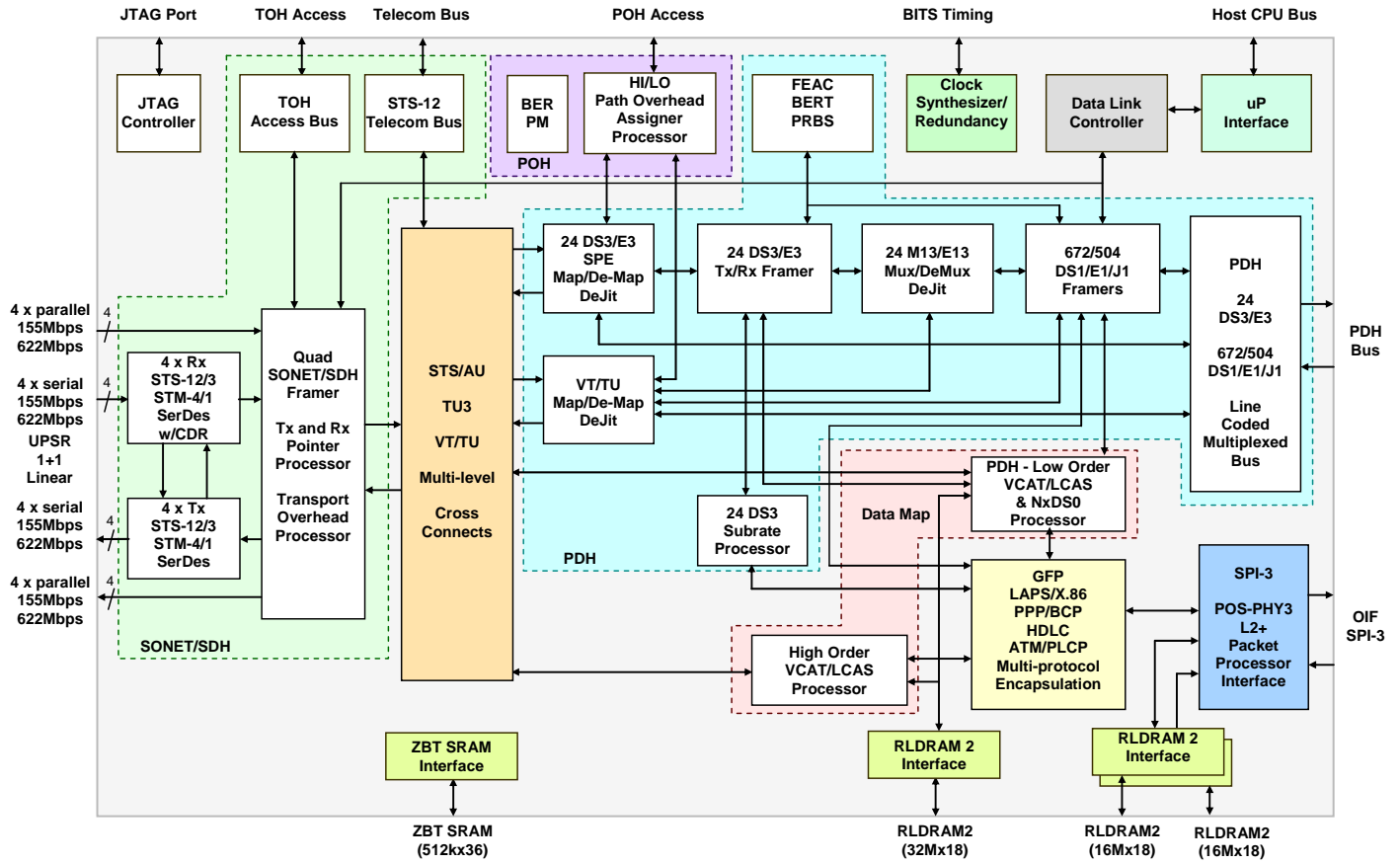
GENERAL FEATURES

- ❑ Provides independently-programmable, channelized network interfaces for 4xOC-12/3 or STM-4/1s with loop-timed capability
- ❑ Flexible diagnostic via network side or line side loopbacks with BERT and detection capabilities
- ❑ High and low-order path overhead (POH) processor
- ❑ Supports hardware-based SONET/SDH automatic protection switching (APS) and SDH Multiplex Section Protection (MSP) for UPSR/SNCP rings, Linear and P2P
- ❑ BER monitor for SONET/SDH lines (including PDH lines)
- ❑ BER monitor for high and low-order POH
- ❑ SONET/SDH overhead add/drop port
- ❑ SONET/SDH cross connect at the STS/AU, TU3 and VT/TU levels allows flexible line or local loopbacks for all PDH payloads
- ❑ Parallel 622Mbps Telecom Bus for STS-12 deep channelized down to DS_n streams
- ❑ Provides ECC on all critical internal RAMs to protect against Soft Errors
- ❑ Supports ECC on all external RAMs to protect against Soft Errors
- ❑ Clock synthesis and network synchronization for local (internal clock) or loop timing (recovered from SONET/SDH network or PDH tributary) or BITS
- ❑ Meets Telcordia and ITU Jitter generation and tolerance requirements
- ❑ External PDH interface Mux/DeMux FPGA design is available from Arrive for interfacing with commercial DS3/E3/DS1/E1 LIUs
- ❑ DS1/E1 framers are implemented with a 672/504 channel framer engine. Each channel can be programmed for DS1, E1 or J1 with any of the supported framing formats. The channel capacity ranges from 504 to 672 based on the 2xOC-12/STM4 mapping capacity
- ❑ The 2048 data encapsulation channels can be randomly assigned to any of the 2048 nxDS0, 672/504 DS1/J1/E1, 24 DS3s/E3, 336 VCAT channels limited by the 2xOC-12/STM-4 aggregate bandwidth and channel limits
- ❑ Implemented in .13u TSMC process
- ❑ Europa is provided in a FCBGA 1296 package
- ❑ Estimated power consumption is 6w

CHANNELIZATION FEATURES

- ❑ Supports termination of 2048 channels
- ❑ Supports un-channelized and channelized DS3/E3
- ❑ Supports DS3 Subrate and Scrambling interoperable with Quickeagle (DigitalLink), Kentrox, Adtran, Verilink and Larscom (CSU/DSUs)
 - Programmable to allow for other subrate methods
- ❑ Supports DS1 clear-channel, framed fractional (including J1)
- ❑ Supports E1 clear-channel, framed fractional and unframed
- ❑ Provides channelization to DS1 to/from SONET:
 - Support for VT1.5 mapping:
STS-12 <-> STS-1 <-> VT1.5 <-> DS1
 - Support for asynchronous DS3, channelized down to DS1 (M13 and C-bit framing) mapped into:
STS-12 <-> STS-1 <-> DS3 <-> DS1
- ❑ Provides channelization to DS1 to/from SDH: STM-4 <-> AU-4 <-> TUG-3 <-> TUG-2 <-> TU-11 <-> VC-11 <-> DS1
- ❑ Provides channelization to E1 to/from SONET:
 - Support for VT2 mapping:
STS-12 <-> STS-1 <-> VT Group <-> VT2 <-> E1
 - Support for asynchronous DS3, channelized down to E1 (M13 framing) mapped into:
STS-12 <-> STS-1 <-> DS3 <-> E1
- ❑ Provides channelization to E1 to/from SDH:
 - Support for ITU-T G.707 (SDH CEPT/ETSI) VC-12 mapping: STM-4 <-> AU-4 <-> TUG-3 <-> TUG-2 <-> TU-12 <-> VC-12 <-> E1
- ❑ Provides channelization to J1 to/from SDH:
 - Support for ITU-T G.707 (SDH-ANSI) VC-11 mapping: STM-4 <-> AU-3 <-> VC-3 <-> TUG-2 <-> TU-11 <-> VC-11 <-> J1
- ❑ Provides channelization to DS3 to/from SONET: STS-12 <-> STS-1 <-> DS3/E3
- ❑ Provides channelization to DS3 to/from SDH:
 - STM-4 <-> AU-3 <-> VC-3 <-> DS3/E3
 - STM-4 <-> AU-4 <-> TUG-3 <-> TU-3 <-> VC-3 <-> DS3/E3
- ❑ Supports 16128 DS0s over up to 2048 NxDS0/E0 channels
 - Each DS1/E1 may be further channelized into NxDS0/E0 channels where N=1-24 for DS1 and N=1-31 for E1
 - DS0s are extracted from Byte Synchronous VT/TUs directly or derived from converted Asynchronous DS1/E1s via internal framers
 - Provides channelization to DS0/E0 (56K or 64K), including multiple channel groupings per DS1/E1 and fractional DS1/E1

BLOCK DIAGRAM





FEATURES SUMMARY

SONET/SDH Features

- ❑ Provides independently-programmable, channelized network interfaces for 4xOC-12/3 or STM-4/1s with loop-timed capability
- ❑ Each OC-12/3 or STM-4/1 interface can be serial with on-chip CDR or parallel via 8-bit data with clock
- ❑ Independent Clocking modes for each transmit STS/VC including
 - Derived from corresponding receive STS/VC
 - Derived from any of SONET/SDH lines
 - Internal generation by the Europa system clock
- ❑ Full SONET/SDH Section/Line Overhead processing
- ❑ Hardware based APS-L processing for Linear/BLSR
- ❑ Hardware based UPSR/SNCP and BPSR/MSSP processing
- ❑ Standard Contiguous and any Random Hi-order and Lo-order pointer processing and alignment
- ❑ Full STS/VC and VT/TU Path monitoring/termination through a selectable 511-channel pool
- ❑ Full SONET/SDH Line 10^{-3} to 10^{-9} hardware BER detection
- ❑ Selectable 511 STS/VC, VT/TU with 10^{-3} to 10^{-9} hardware BER detection
- ❑ Full TOH and flexible 64 POH channels add/drop port
- ❑ Selectable 128 STS-1 Transport Overhead (TOH) Transparency
- ❑ Hitless backplane switching

Cross-Connect Features

- ❑ Provides multi-level cross-connection
- ❑ Non-blocking STS/AU/VT/TU for OC-12/STM-4 ADM applications
- ❑ STS/AU cross-connect
 - Full, non-blocking cross-connect for STS-1/VC-3 level
 - STS/VC path select for UPSR/SNCP
 - Multicast and broadcast on per STS-1/VC-3 basis
- ❑ TU3 cross-connect
 - Full, non-blocking cross-connect for TU3s
 - Supports TU3 path select for UPSR/SNCP application
 - Supports multicast and broadcast on per TU3 basis
 - Provides DS3/E3 payload loopbacks in and out, plus flexible diagnostic arrangements for BERT testing
- ❑ VT/TU cross-connect
 - Full, non-blocking cross-connect for VT1.5/TU11/VT2/TU12s
 - Supports cross-connect for all types of VT/TU
 - Supports VT/TU path select for UPSR/SNCP application
 - Supports multicast and broadcast on per VT1.5/TU11/VT2/TU12 basis
 - Provides DS1/E1/J1 payload loopbacks in and out, plus flexible diagnostic arrangements for BERT testing

DS3 Features

- ❑ Up to 24 DS3 framers
- ❑ Supports C-bit parity or M23 framing with channelized, clear-channel or subrate
- ❑ Independent Clocking modes for each transmit DS3 including
 - Derived from corresponding receive DS3
 - Derived from any of SONET/SDH lines
 - Internal generation by the Europa system clock
- ❑ Loopback capabilities:
 - Remote line loopback
 - Remote payload loopback
 - Local line loopback
 - Local payload loopback
- ❑ Supports loopback detection/insertion
 - DS3 FEAC channel for C-bit parity
 - C-bit inversion for M23
- ❑ BERT generator and detector at DS3 level including
 - PRBS 9/11/15/20/23 (inverted or not)
 - A configurable fixed pattern which is selectable from 1-bit to 32-bit
- ❑ Local and remote performance monitoring
- ❑ Detect and insert BOC (Bit Oriented Commands)
- ❑ Alarm and event detection: AIS, RDI, LOS and LOF (Near-End And Far-End), LOMF (Loss Of Multi-Frame)
- ❑ Un-channelized DS3 supporting subrate and scrambling formats for Quickeagle (DigitalLink), Kentrox, Adtran, Verilink and Larscom (CSU/DSUs)

E3 Features

- ❑ Up to 24 E3 framers
- ❑ Supports ITU-T G.751 or G.832 framing with channelized or clear-channel
- ❑ Independent Clocking modes for each transmit E3 including
 - Derived from corresponding receive E3
 - Derived from any of SONET/SDH lines
 - Internal generation by the Europa system clock
- ❑ Loopback capabilities:
 - Remote line loopback
 - Remote payload loopback
 - Local line loopback
 - Local payload loopback
- ❑ Loopback modes: DTE, local, dual, and network
- ❑ BERT at E3 level including
 - PRBS 9/11/15/20/23 (inverted or not)
 - A configurable fixed pattern which is selectable from 1-bit to 32-bit
- ❑ Performance data collection
- ❑ Framing pattern errors accumulation
- ❑ BIP-8 error counts (Path-Parity Errors)
- ❑ Far-End Block Error (FEBE) counts
- ❑ E3 alarm/event detection: AIS, LOF, RAI, OOF, FERF



DS1 Features

- ❑ Up to 672 DS1 framers
- ❑ Supports SF/ESF/SLC-96/DDS framing
- ❑ Supports J1 SF/ESF framing
- ❑ Independent Clocking modes for each transmit DS1 including
 - Derived from corresponding receive DS1
 - Derived from any of SONET/SDH lines
 - Internal generation by the Europa system clock
- ❑ Loopback capabilities:
 - Remote line loopback
 - Remote payload loopback
 - Local line loopback
 - Local payload loopback
- ❑ Supports loopback detection/insertion
 - Inband loopcode on DS1 payload, full DS1 or DS1 with F-bit overwrite
 - FDL channel
- ❑ Error and alarm detection: CRC errors, framing errors, LOF (red), AIS (blue), RAI (yellow)
- ❑ BERT generator and detector at DS1 level including
 - QRSS, PRBS 9/11/15/20/23 (inverted or not), DDS1/2/3/4/5, Fix 3 in 28, Fix 1 in 8, DALY/55 Octet
 - A configurable fixed pattern which is selectable from 1-bit to 32-bit
- ❑ ANSI T1.403 facility data link (FDL) on ESF mode and AT&T 54016 FDL mode
- ❑ Local and remote performance monitoring (PM)
- ❑ Detect and insert BOC (Bit Oriented Commands)
- ❑ Alarm and event detection: AIS, RDI, LOS and LOF (Near-End And Far-End), LOMF (Loss Of Multi-Frame)

E1 Features

- ❑ Up to 504 E1 framers
- ❑ Framing: CRC-4 and non-CRC-4 conformance with ITU-T G.704
- ❑ Independent Clocking modes for each transmit E1 including
 - Derived from corresponding receive E1
 - Derived from any of SONET/SDH lines
 - Internal generation by the Europa system clock
- ❑ Loopback capabilities:
 - Remote line loopback
 - Remote payload loopback
 - Local line loopback
 - Local payload loopback
- ❑ Error and alarm detection: CRC errors, framing errors, LOF, AIS, RAI (Remote Alarm Indication)
- ❑ BERT generator and detector at E1 level including
 - QRSS, PRBS 9/11/15/20/23 (inverted or not), DDS1/2/3/4/5, Fix 3 in 28, Fix 1 in 8, DALY/55 Octet
- ❑ A configurable fixed pattern which is selectable from 1-bit to 32-bit

DS0 Signaling Processor

- ❑ Up to 16128 DS0s
- ❑ Signaling processor for ABCD signaling scan
- ❑ Signaling de-bounce
- ❑ Signaling freeze and signaling conversion

Data Encapsulation Features

- ❑ ATM, GFP, PPP/HDLC, LAPS simultaneously, full-duplex for 2048 data channels
- ❑ GFP/HDLC/PPP/BCP/LAPS/ATM mapping to PDH in compliance with G.8040, X.85/86, G.804 and IEEE 802.6
- ❑ Supports direct ATM cell mapping for STS/VC, VT/TU, DS1, E1, DS3, E3 and NxDS0
- ❑ Supports ATM direct mapping or PLCP for 24xDS3/E3
- ❑ Supports Cisco HDLC
- ❑ Supports Frame Relay mapping
- ❑ Supports Inverse Multiplexing over ATM (IMA) across PDH with the assistance of an external Network Processor
- ❑ Supports Multilink Frame Relay (ML FR), Multilink Point-to-Point Protocol (ML PPP) with the assistance of an external Network Processor
- ❑ Complies with ITU-T I432.2 (ATM), ITU-T G.7041 (GFP), RFC-1619/1662/2615 (PPP), ITU-T X.85/86 (LAPS), HDLC mapping standards
- ❑ Supports transparent mode to pass STS/VC, VT/VC, DS1/E1/DS3/E3 through the SPI interface
- ❑ Cell HEC and packet FCS checker/generator and 1-bit HEC error correction
- ❑ Idle/unassigned cell and aborted sequence detection/generation
- ❑ Cell/packet payload scrambling/de-scrambling
- ❑ Supports 16 or 32 bit frame check sequence field (FCS) per channel data
- ❑ Supports GFP-F with double configuration FCS generation and checking for GFP and FCS Ethernet/PPP
- ❑ Supports ATM idle cell discard or pass-through
- ❑ Bit stuffing and byte stuffing on PPP and HDLC
- ❑ Extraction and insertion header field support
- ❑ Supports frame extraction and insertion
- ❑ Various statistic events per GFP data channel
 - Good frame counters on transmit and receive
 - cHEC, tHEC, eHEC uncorrected error counters
 - FCS error counters
 - Frame drop/discard event counters
 - Idle frame counter on receive
 - Transmit underrun counter
 - Transmit unexpected length error counter
 - Out of frame delineation event



Encapsulation Features (Cont.)

- ❑ Various statistic events per ATM data channel
 - Good cell counters on transmit and receive
 - HEC uncorrected error counters
 - Single bit HEC error correction counter
 - Cell drop/discard event counters
 - Idle cell counter on receive
 - Transmit underrun counter
 - Out of cell delineation (OCD) event
 - Loss of cell delineation (LCD) event
 - Receive PLCP BIP errors
 - Receive PLCP Remote Alarm Detected event
 - Receive PLCP Out of Frame event
- ❑ Various statistic events per HDLC/PPP/BCP/LAPS data channel
 - Good frame counters on transmit and receive
 - FCS error counters
 - Abort sequence detection counter
 - Frame length violation counters on transmit and receive
 - Frame drop/discard event counters
 - Transmit underrun counter

VCAT/LCAS/Data Mapping Features

- ❑ STS/VC, VT/TU, E1/DS1/E3/DS3 termination via 2048 data channels
- ❑ Supports standard-based Contiguous, any Random and Virtual Concatenation for STS/VC and VT/TU level
- ❑ Supports E1/DS1/E3/DS3 VCAT and LCAS in compliance with G.7043
- ❑ Supports up to 336 VCGs for VCAT termination
- ❑ Complies with Link Capacity Adjustment Scheme (LCAS) as in ITU-T G.7042 with hitless addition/removal and fault isolation
- ❑ TUG-3 SDH concatenation with both VC-4-Xv and VC-3-Xv support
- ❑ Contiguous and Random Concatenation with high-order for VC-3-Xc (X=1-24), VC-4-Xc (X=1-8); low-order for VC-2-Xc (X=1-21), VC12-Xc (X=1-28), VC-11-Xc (X=1-7)
- ❑ SONET/SDH with high-order for VC-3-Xv (X=1-24), VC-4-Xv (X=1-8); low-order for VC-2-Xv (X=1-21), VC-12-Xv (X=1-63), VC-11-Xv (X=1-64)
- ❑ PDH VCAT for Nx1544, Nx2048 (N=1-16), Nx34368, Nx44736 (N=1-8)
- ❑ Data mapping over DS1/J1/E1/DS3/E3 in compliance with G.8040, X.85/86, G.804 and IEEE 802.6
- ❑ EoPDH and legacy data mapping-over-PDH and over SONET/SDH

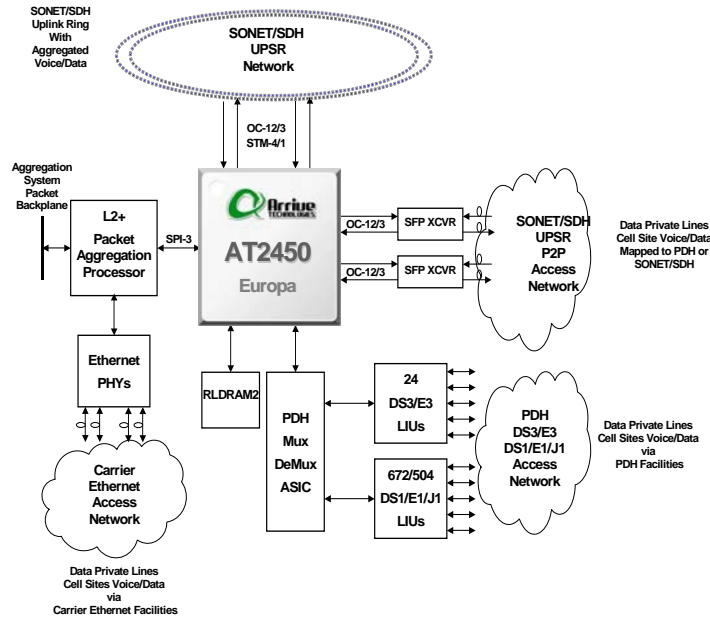
VCAT/LCAS/Data Mapping Features (Cont.)

- ❑ Terminates 16128xDS0 via 2048 data channels
 - Supports Nx64Kbps and Nx56Kbps
 - Supports multiple channel grouping per DS1/E1 and fractional DS1/E1
 - Supports contiguous and non-contiguous NxDS0
 - Supports NxDS0 BERT including
 - o QRSS, PRBS 9/11/15/20/23 (inverted or not), DDS1/2/3/4/5, Fix 3 in 28, Fix 1 in 8, DALY/55 Octet
 - o A configurable fixed pattern which is selectable from 1-bit to 32-bit
 - Supports NxDS0 loopback detection/insertion
 - o Inband user-designed loopcode
 - o Inband $X^7 + X^3 + 1$ loopcode (T1.403-1999)
 - o Loopcode pattern can be detected/inserted from/to 64Kbps or 56Kbps group
- ❑ Accommodates a SONET/SDH VCAT differential delay of 256ms using an external buffer via RLDRAM2
- ❑ Accommodates a PDH VCAT differential delay of 384ms for DS1s, 256ms for E1/E3s, and 217ms for DS3s
- ❑ Optimized low latency in VCAT de-skew
- ❑ On-the-fly programmable differential delays for each VCAT channel to permit short paths and long international paths
- ❑ Supports 256Mbits and 512Mbits RLDRAM2
- ❑ As small as 256Mbits of RLDRAM2 configuration (excluding ECC), Europa can de-skew
 - +/- 64 ms for 512 VC-11/VT-1.5s
 - +/- 85 ms for full 24 VC-3/STS-1s
 - +/- 85 ms for full 24 E3s
 - +/- 72 ms for full 24 DS3s
 - +/- 64 ms for 512 E1s
 - +/- 96 ms for 512 DS1s

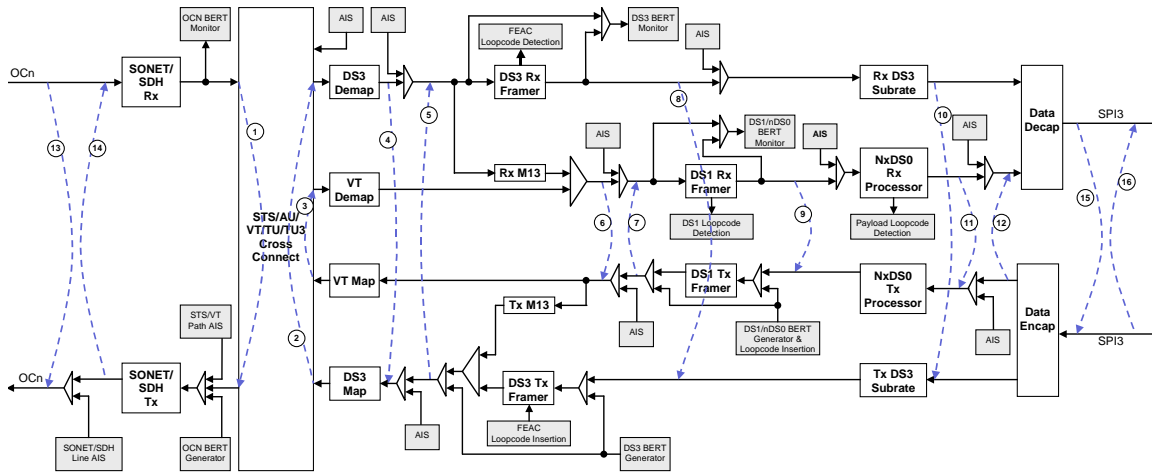
SPI-3 Queue Management Features

- ❑ SPI-3 interface supports a maximum of 2048 data channels over 8 logical ports for transporting data over SONET/SDH
- ❑ Supports interface clock rate from 52MHz to 104MHz
- ❑ Provides 8/16/32-bit interface bus width
- ❑ Programmable 64/128-byte transfer size
- ❑ Provisioning Pre-pended Tag for carrying 11-bit channel ID
- ❑ Dynamic link multiple block buffer to store larger packet; maximum packet size supported is 15KB
- ❑ 2K queues for Rx direction
- ❑ 4K queues for Tx direction with low-priority and high-priority queues per channel
- ❑ Optional discard or transfer error packet through SPI-3 system interface
- ❑ Provides status bus for queue visibility to handle flow control including full, satisfied, hungry and starving statuses

MSPP/WIRELESS/ETHERNET/PDH – AGGREGATION APPLICATION



EUROPA LOOPBACKS



Note:

- (1) STS/AU/TU3/VT/TU Remote Loopback via Cross Connect (all channels concurrently)
- (2) STS/AU/TU3 Local Loopback via Cross Connect (all channels concurrently)
- (3) VT/TU Local Loopback via Cross Connect (all channels concurrently)
- (4) DS3/E3 Remote Line Loopback (all channels concurrently)
- (5) DS3/E3 Local Line Loopback (all channels concurrently)
- (6) DS1/E1/J1 Remote Line Loopback (all channels concurrently)
- (7) DS1/E1/J1 Local Line Loopback (all channels concurrently)
- (8) DS3/E3 Remote Payload Loopback (all channels concurrently)
- (9) DS1/E1/J1 Remote Payload Loopback (all channels concurrently)
- (10) DS3 Substrate Remote Payload Loopback (all channels concurrently)
- (11) Encap/Decap Remote Loopback (selectable 16-channel pool)
- (12) Encap/Decap Local Loopback (selectable 16-channel pool)
- (13) SONET/SDH Remote Line Loopback
- (14) SONET/SDH Local Line Loopback
- (15) Full SPI Bus Remote Loopback
- (16) Full SPI Bus Local Loopback

All AIS functions are supported outside the loopback path.

CHANNELIZED ENCAPSULATION

